

FIG. 1

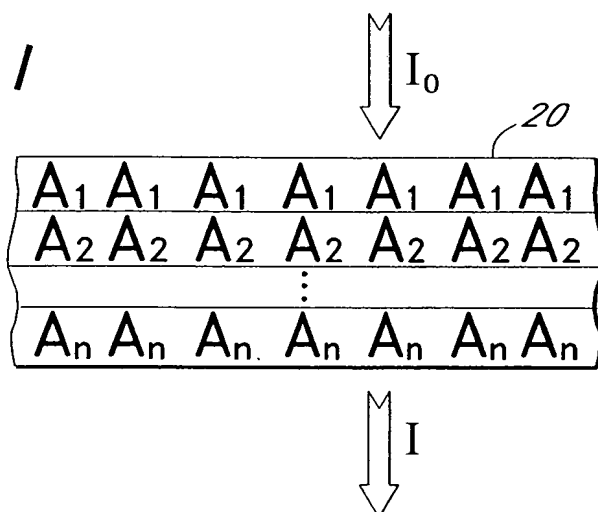


FIG. 2a

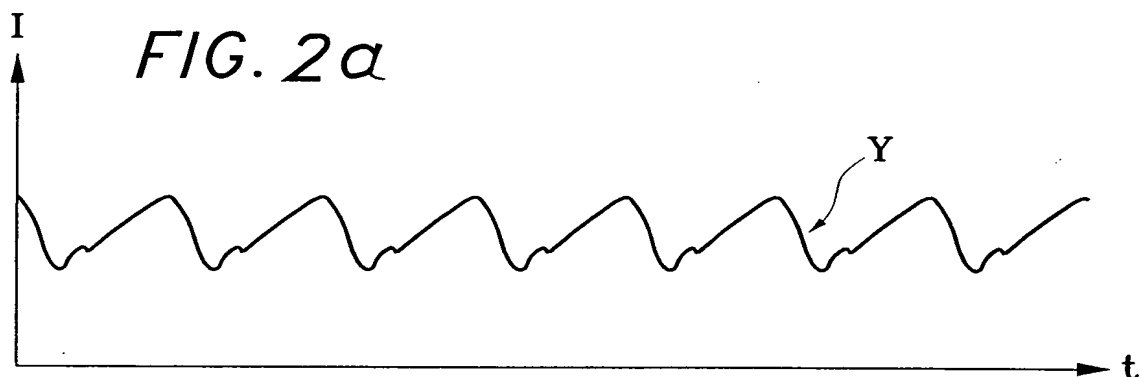


FIG. 2b

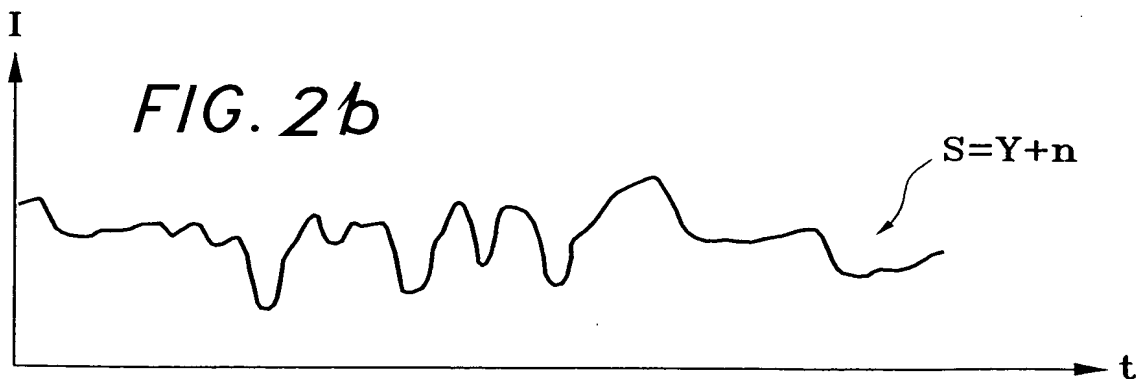


FIG. 3

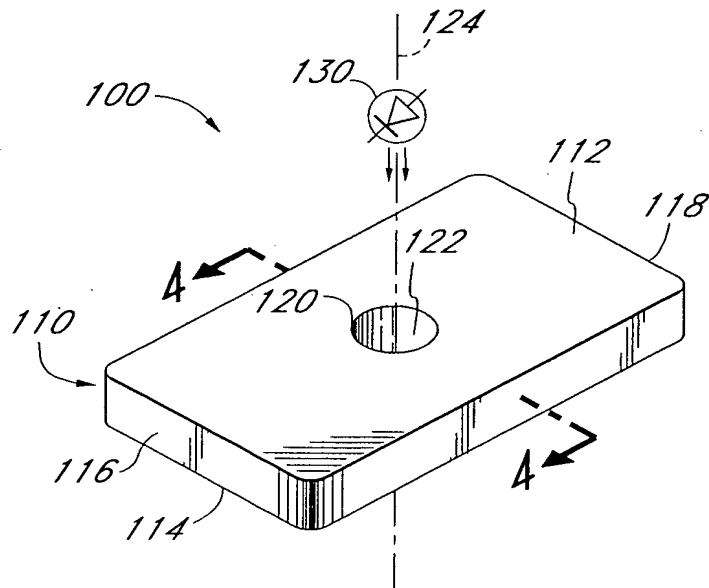


FIG. 4

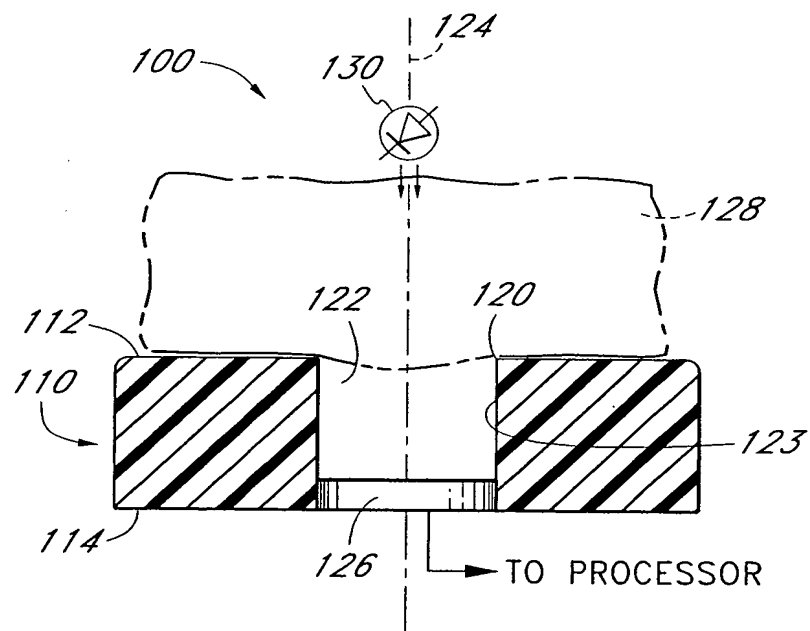


FIG. 5

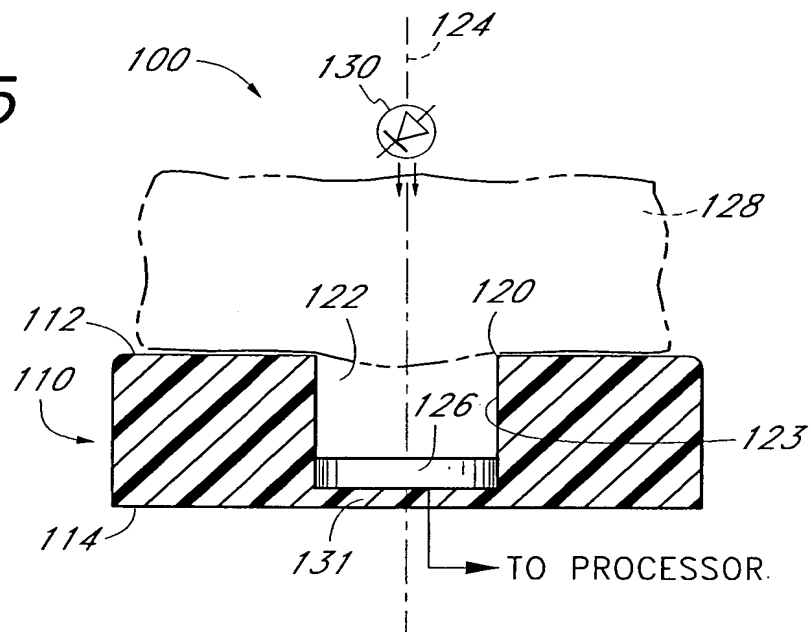
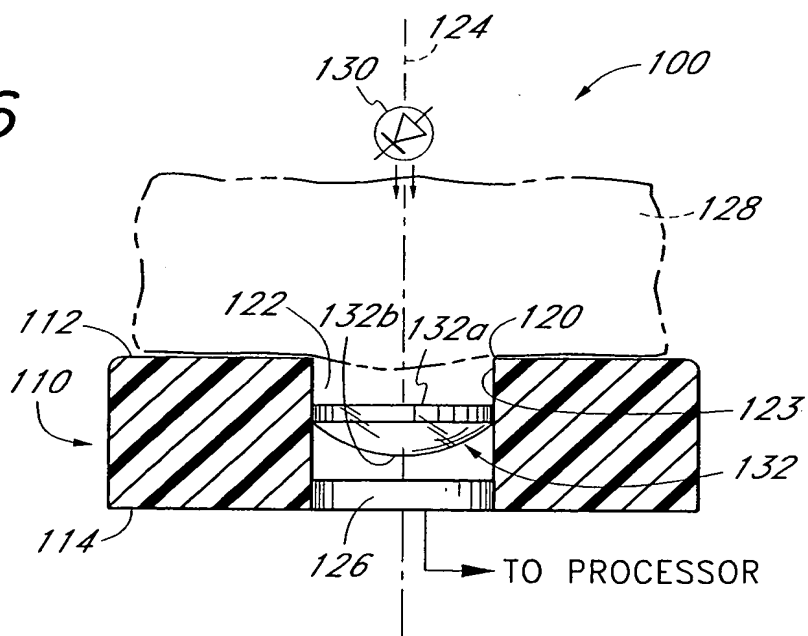


FIG. 6



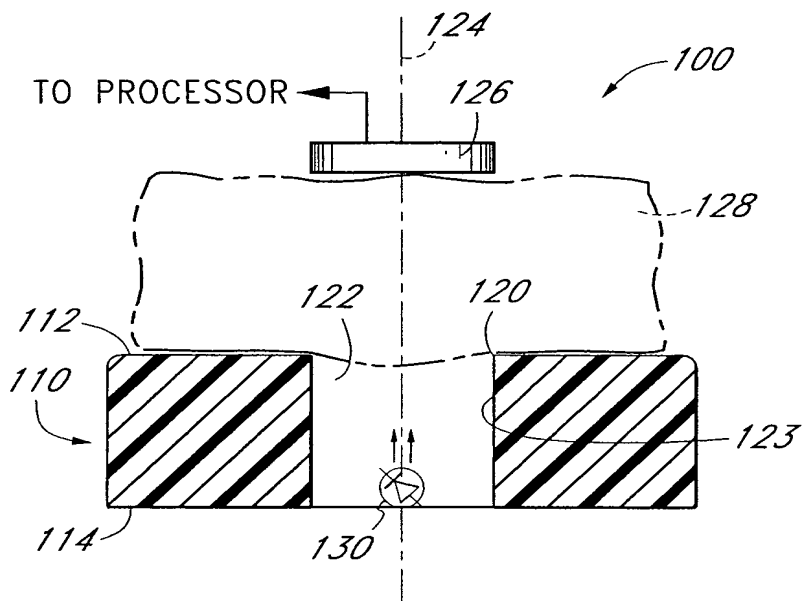


FIG. 7

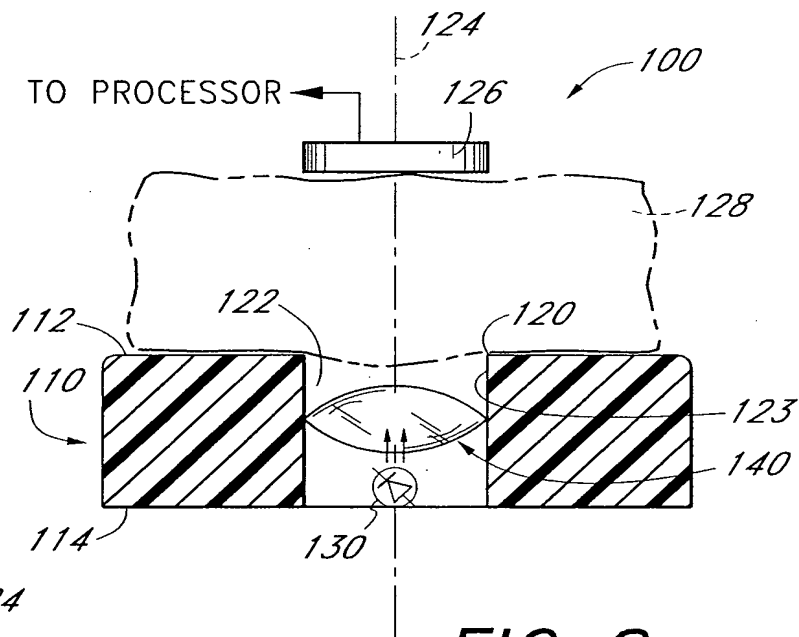


FIG. 8

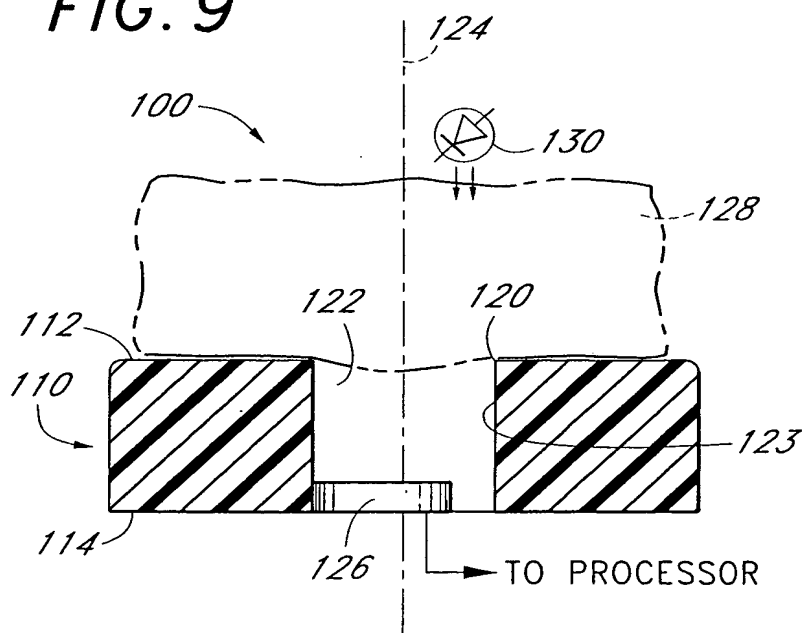


FIG. 9

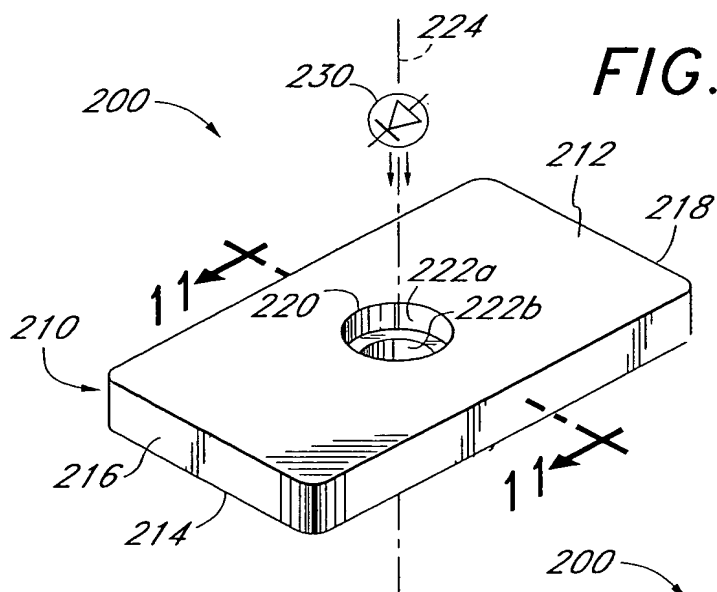


FIG. 10

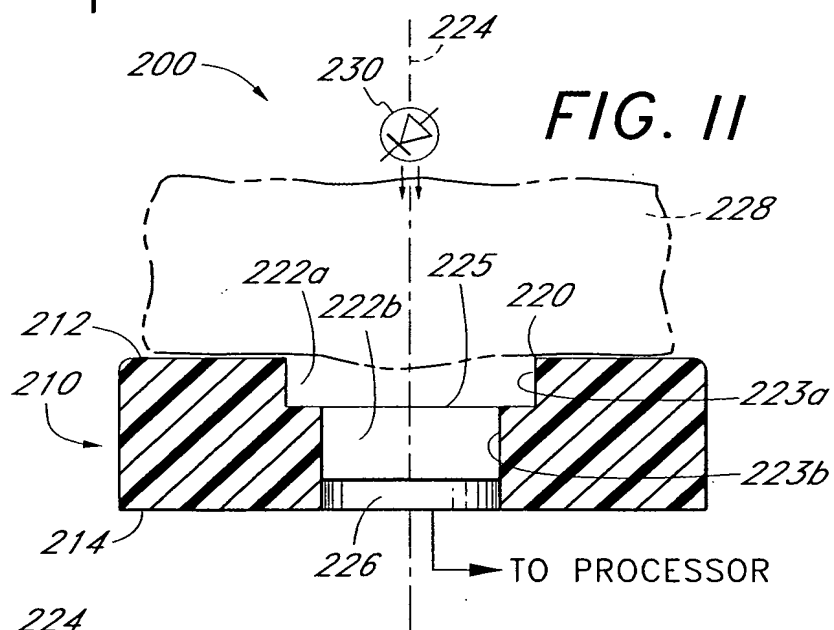


FIG. 11

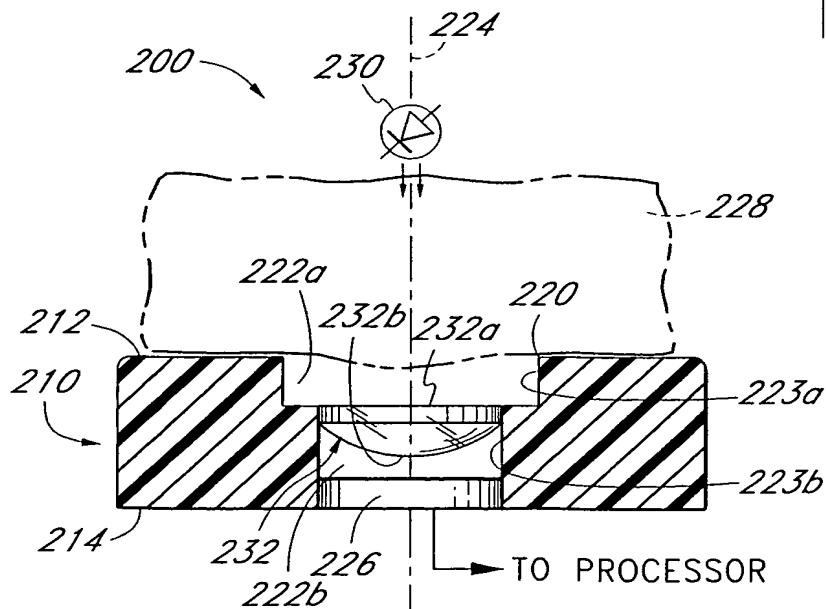


FIG. 12

FIG. 13

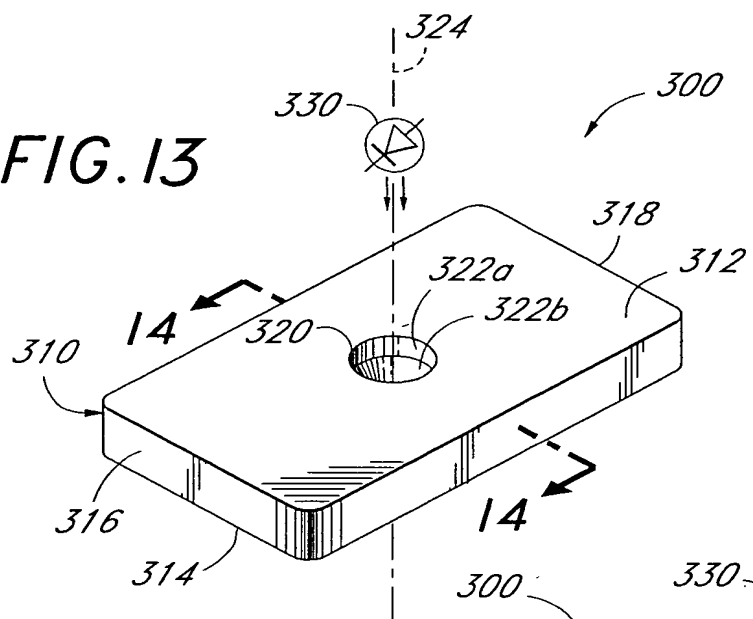


FIG. 14

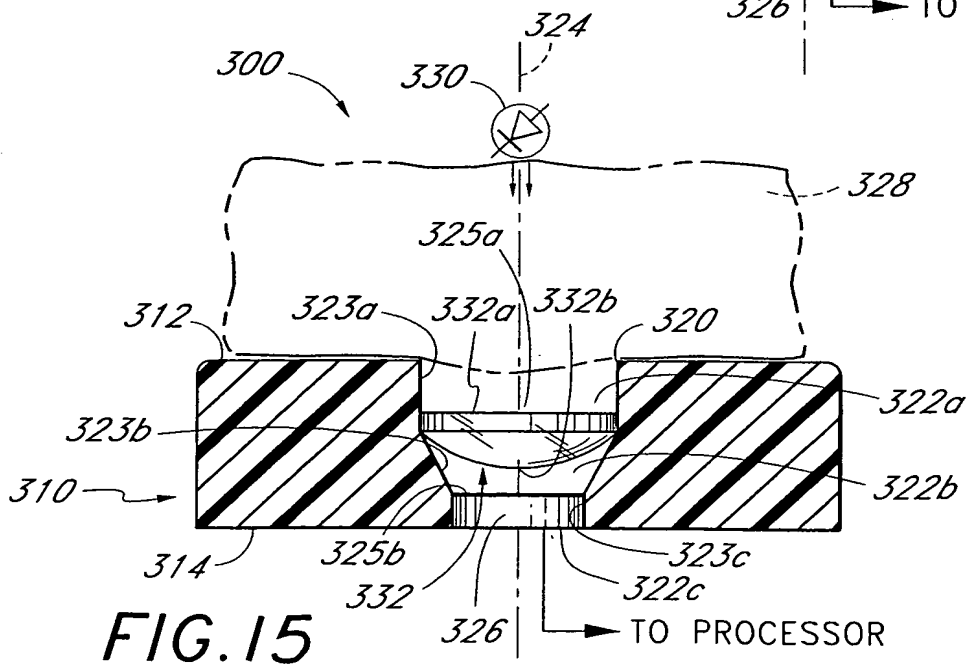
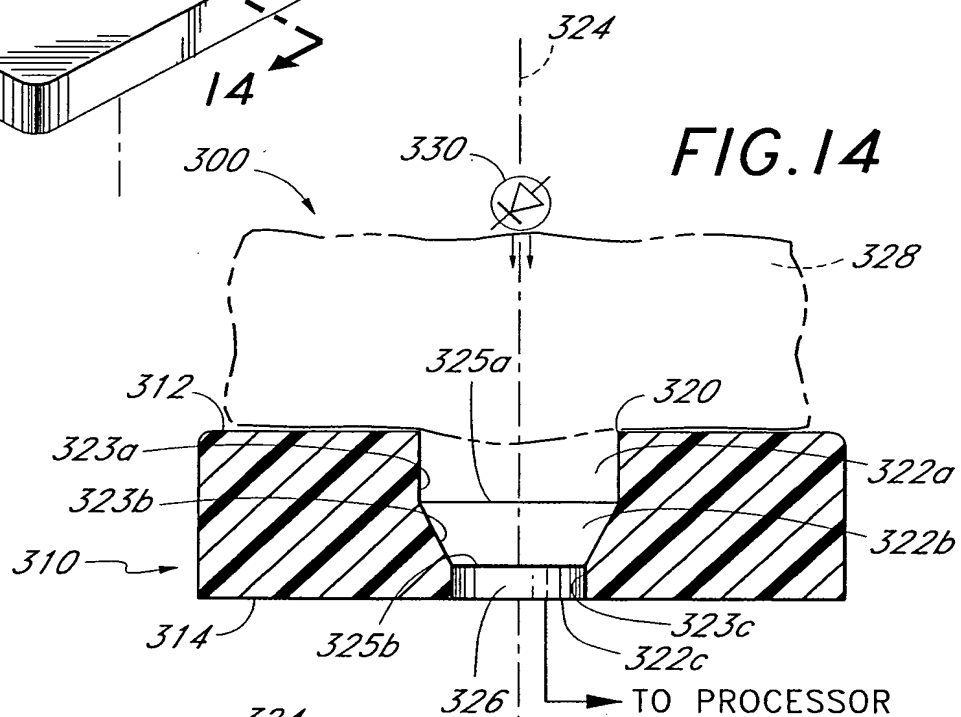


FIG. 15

FIG. 16

FIG. 16

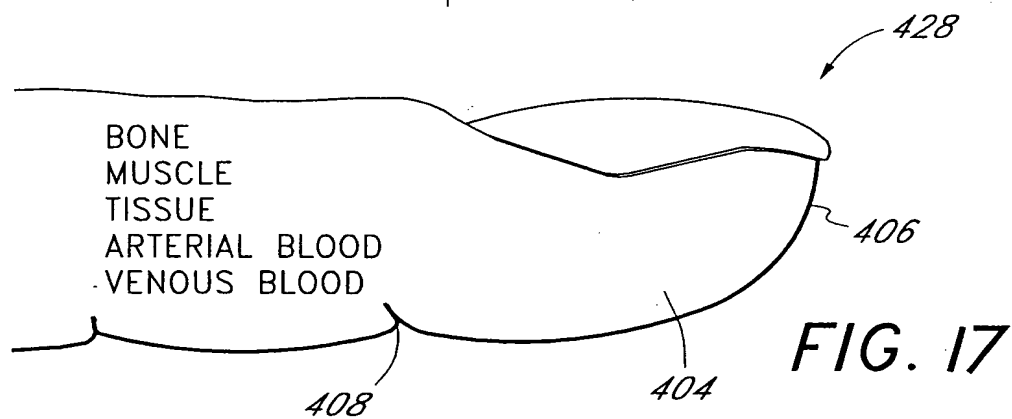
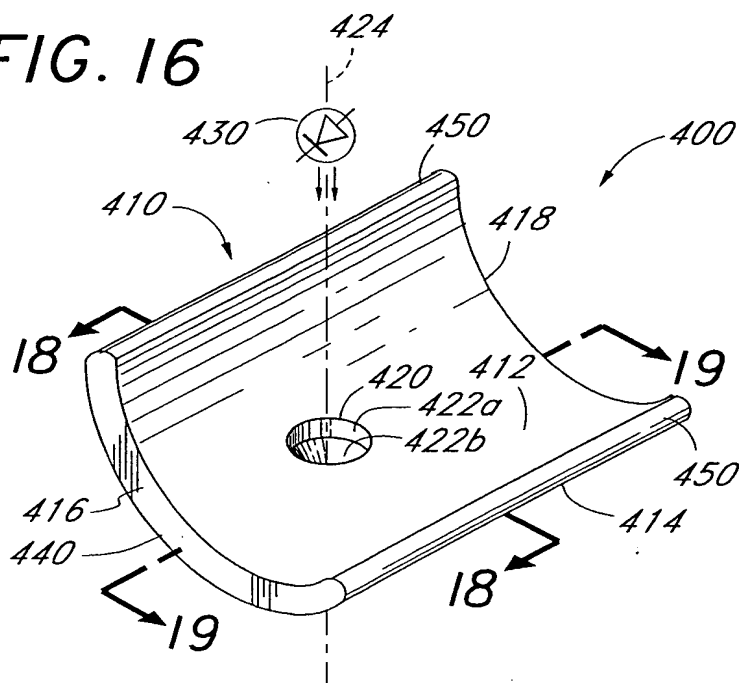


FIG. 17

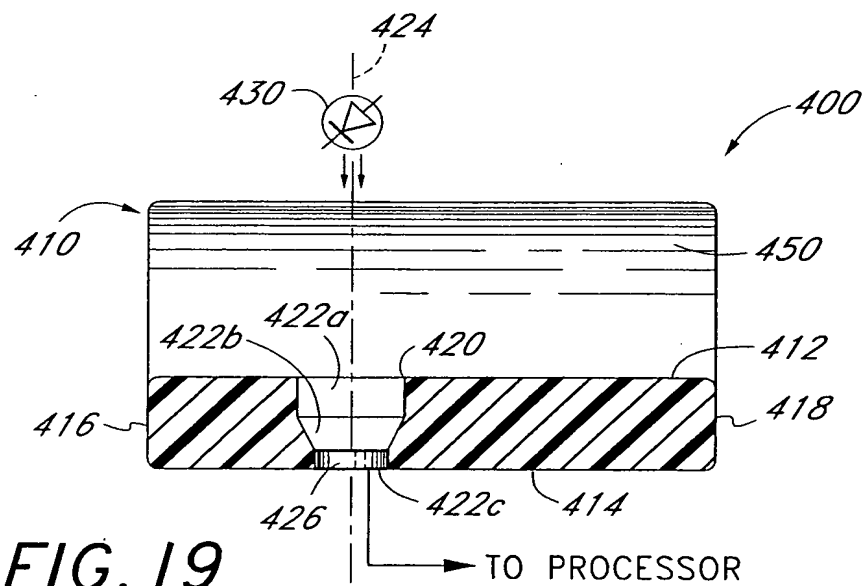


FIG. 19

TO PROCESSOR

FIG. 18

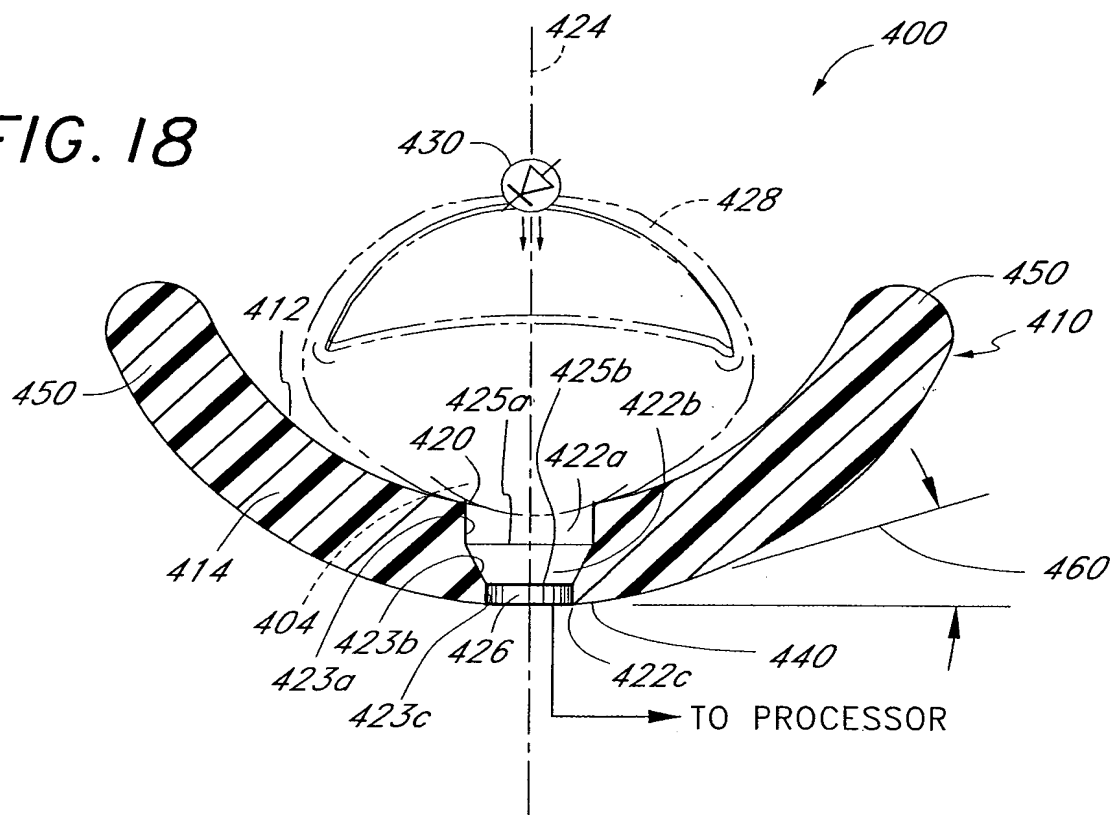


FIG. 20

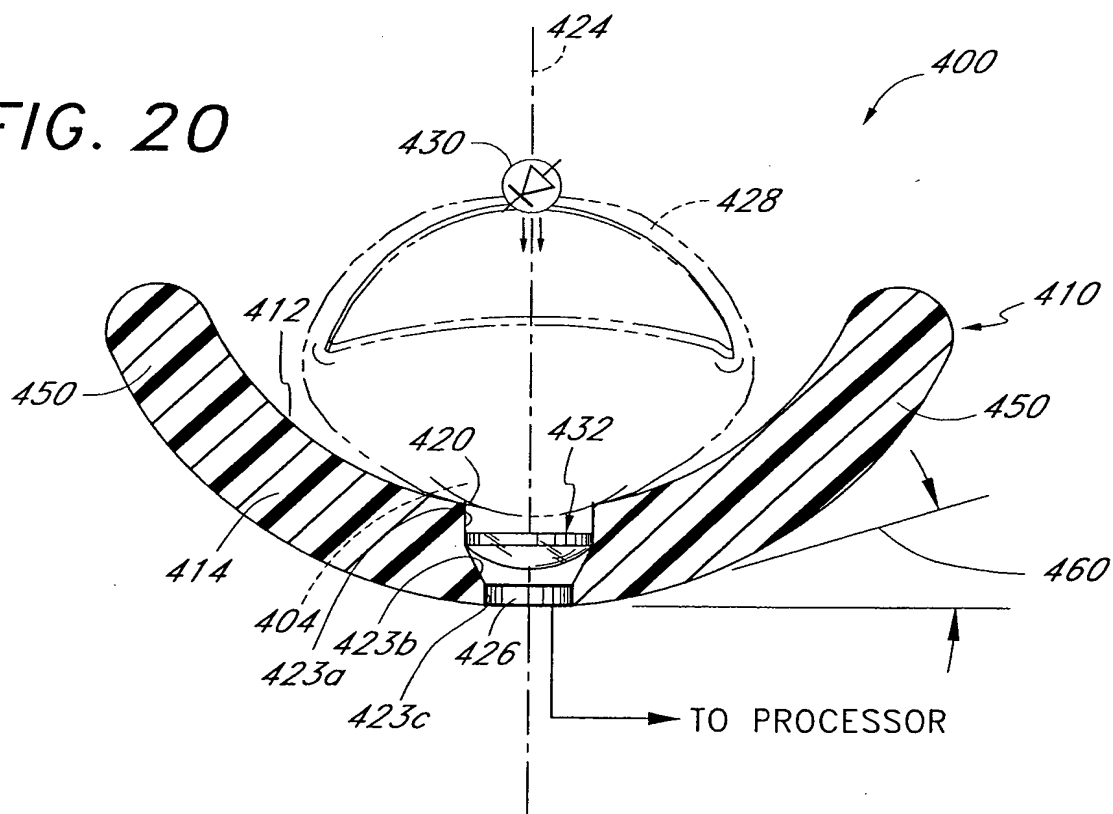


FIG. 21

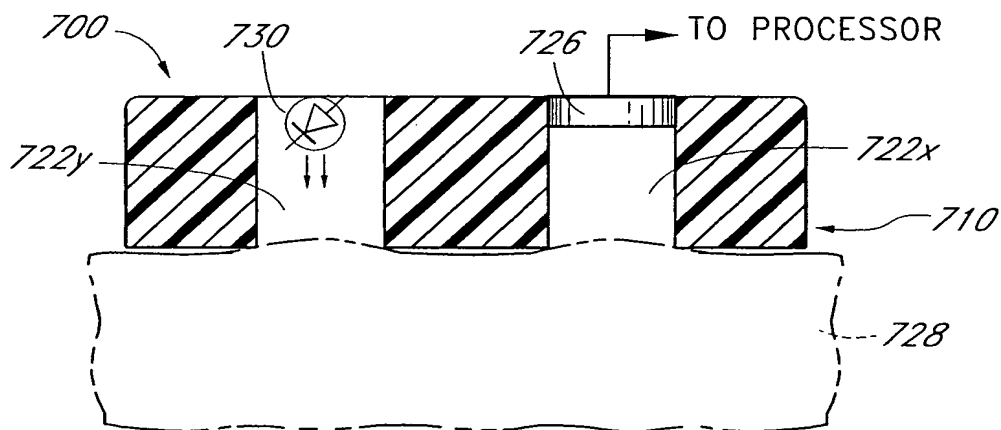


FIG. 22

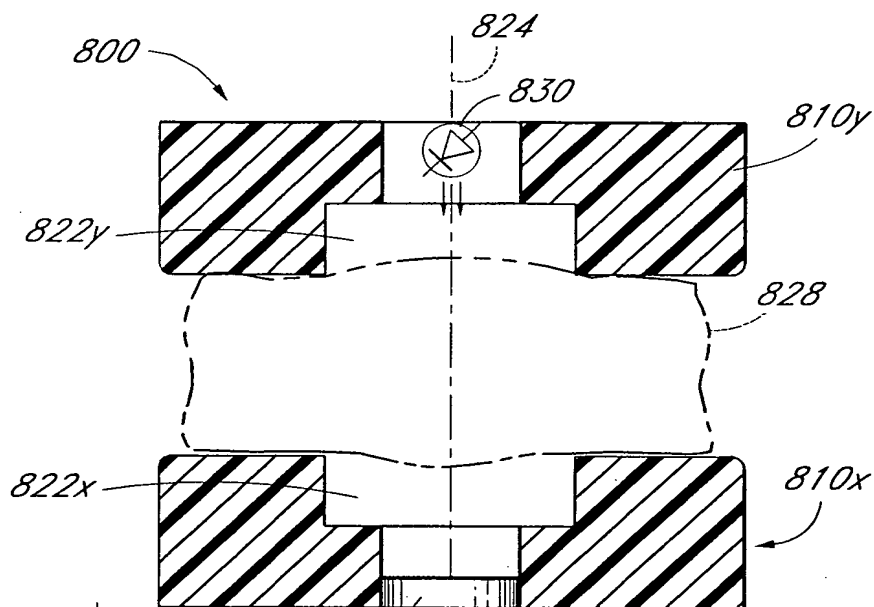
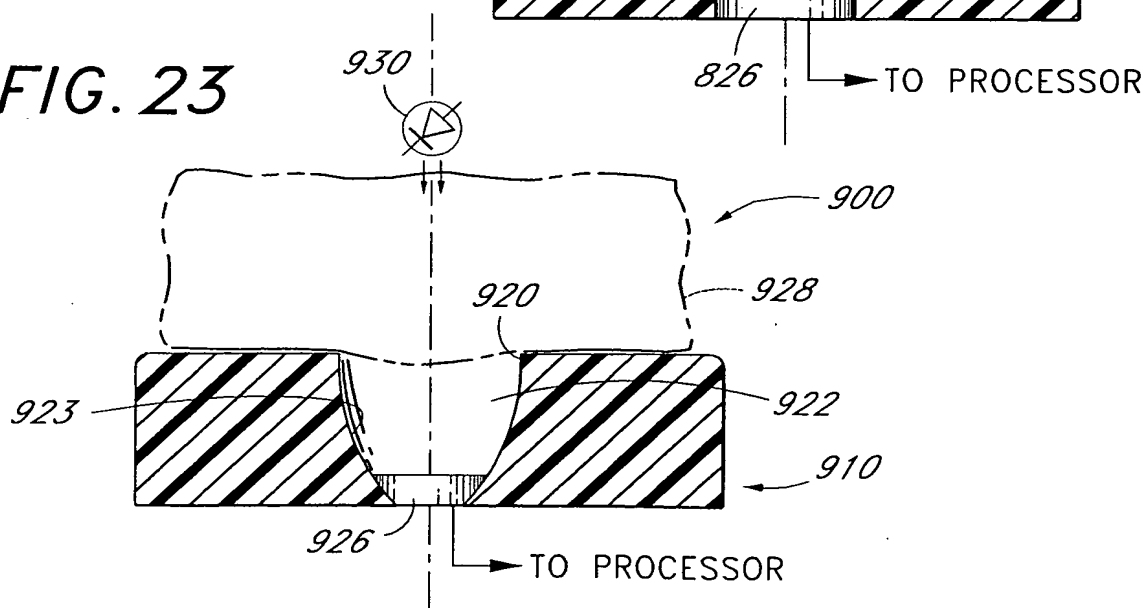


FIG. 23



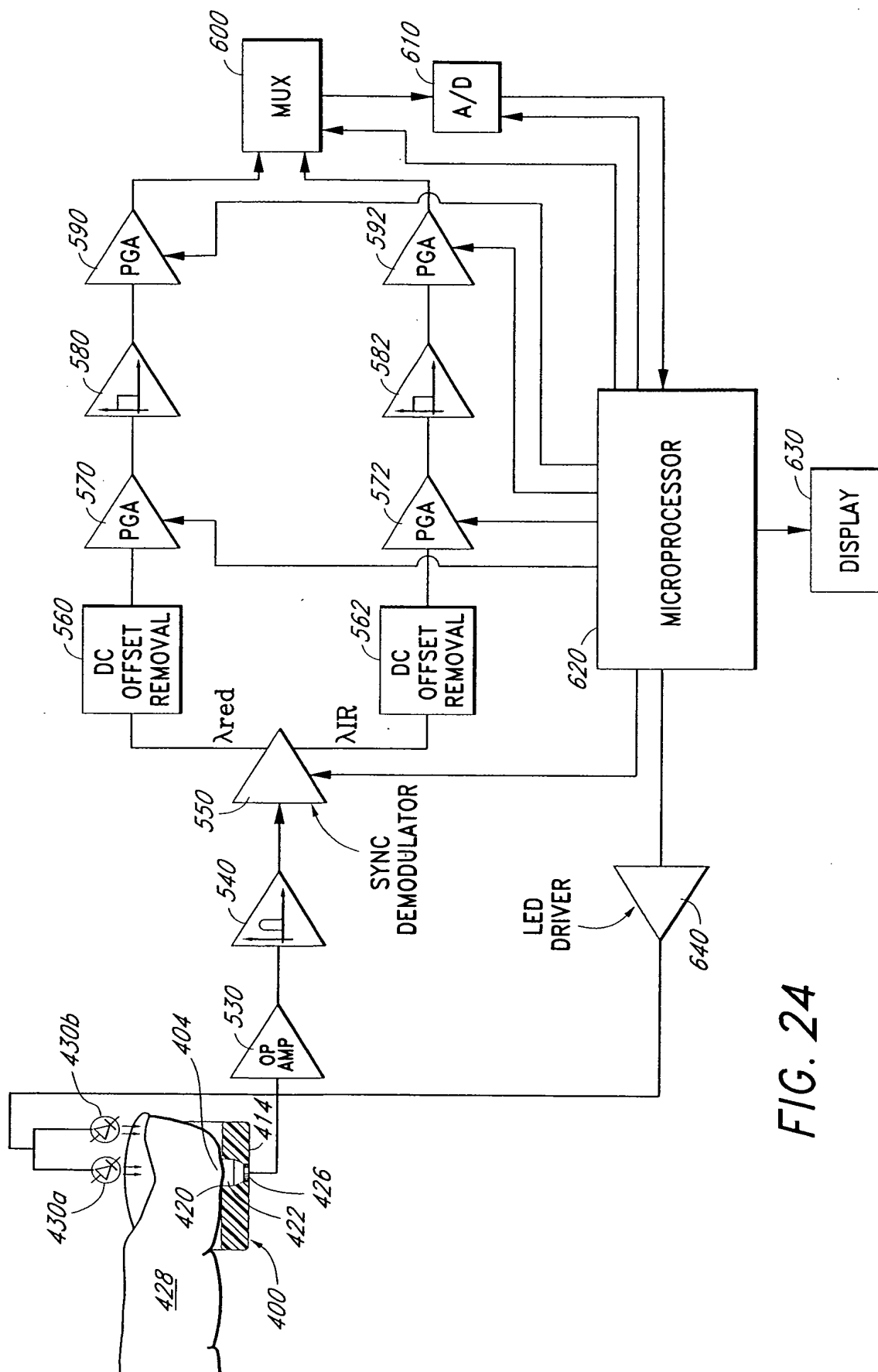


FIG. 24

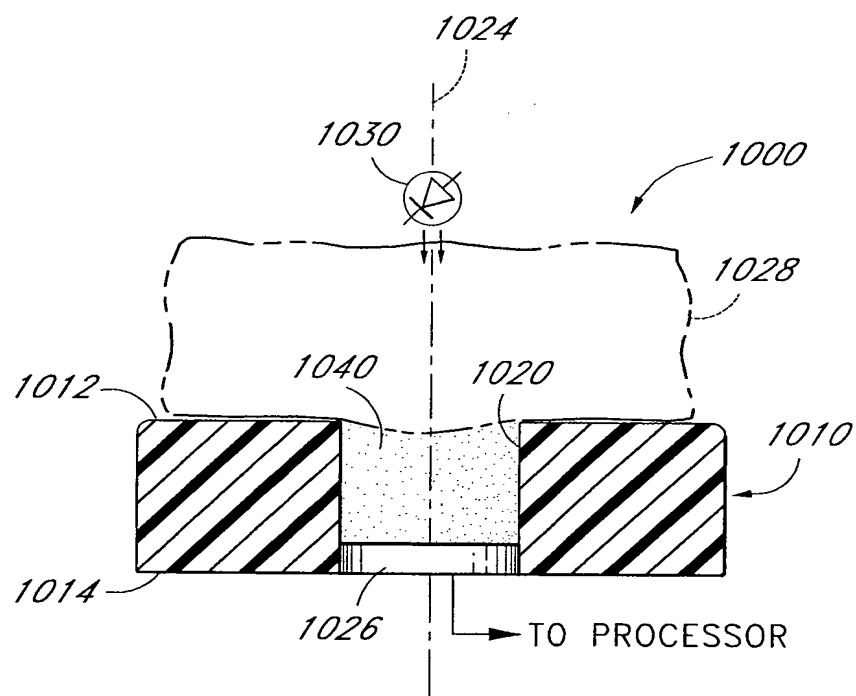
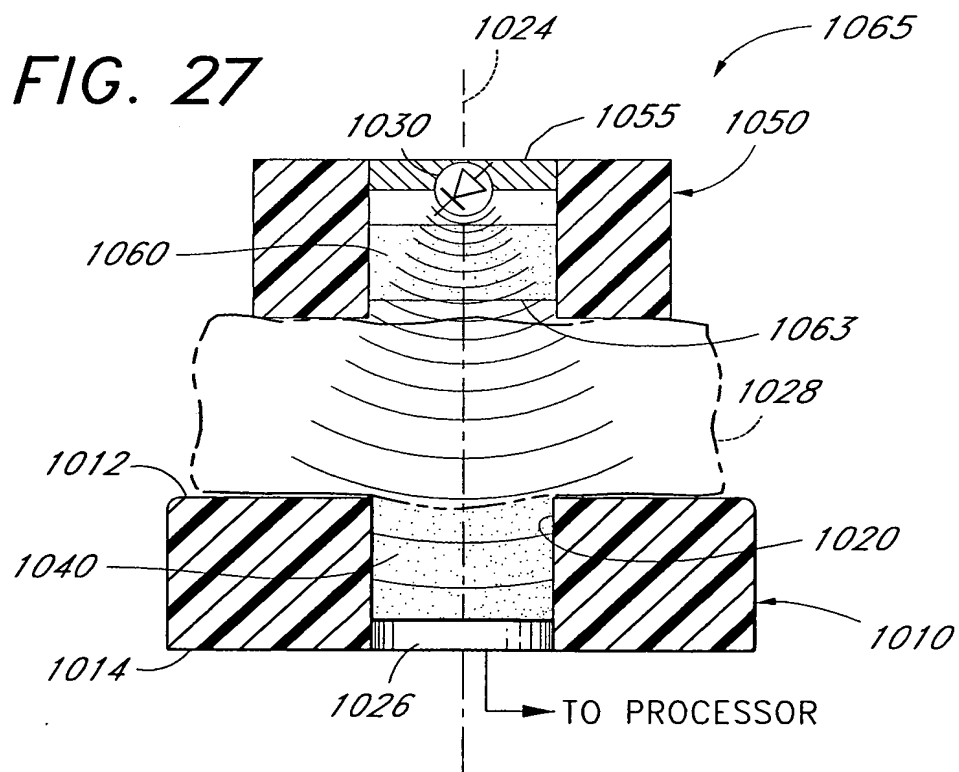
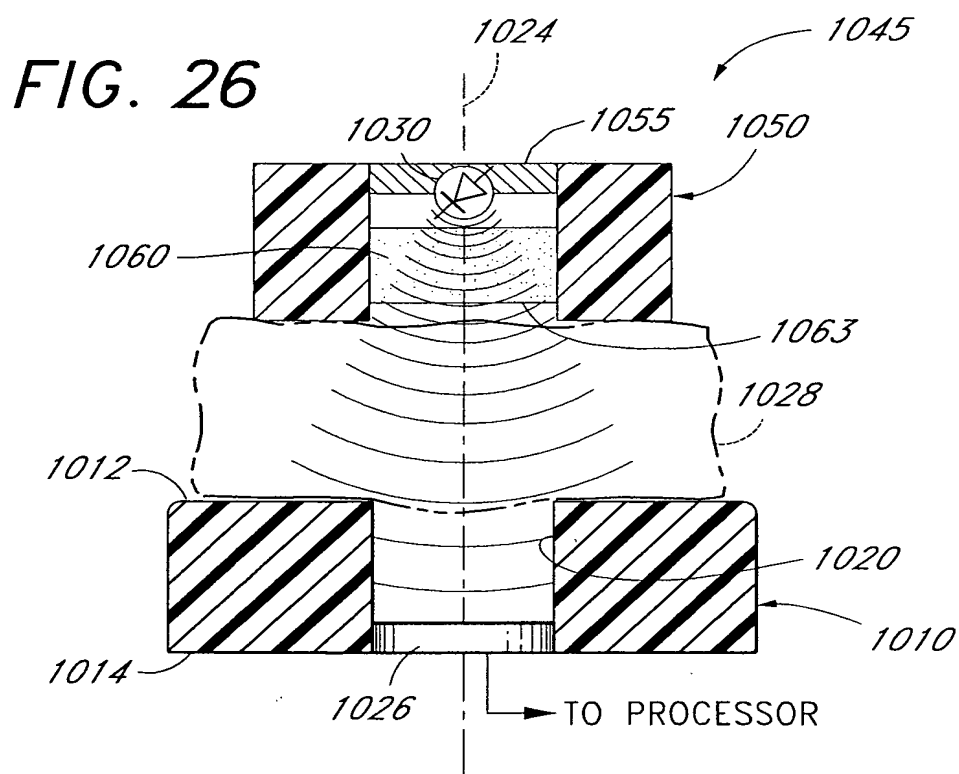


FIG. 25



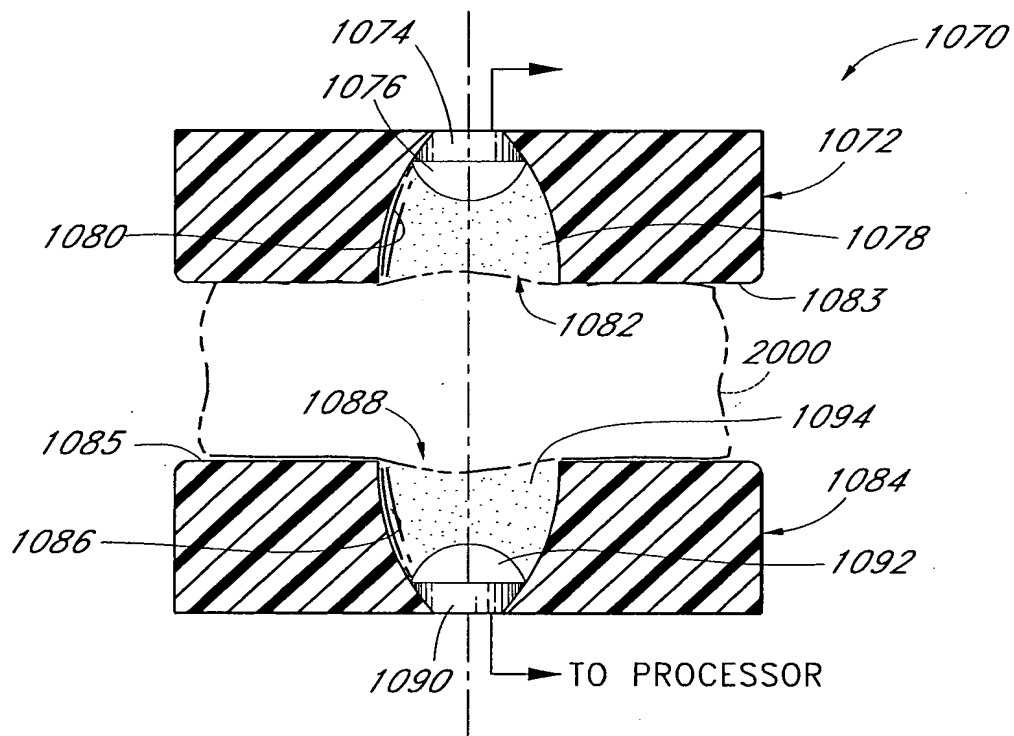


FIG. 28

FIG. 29A

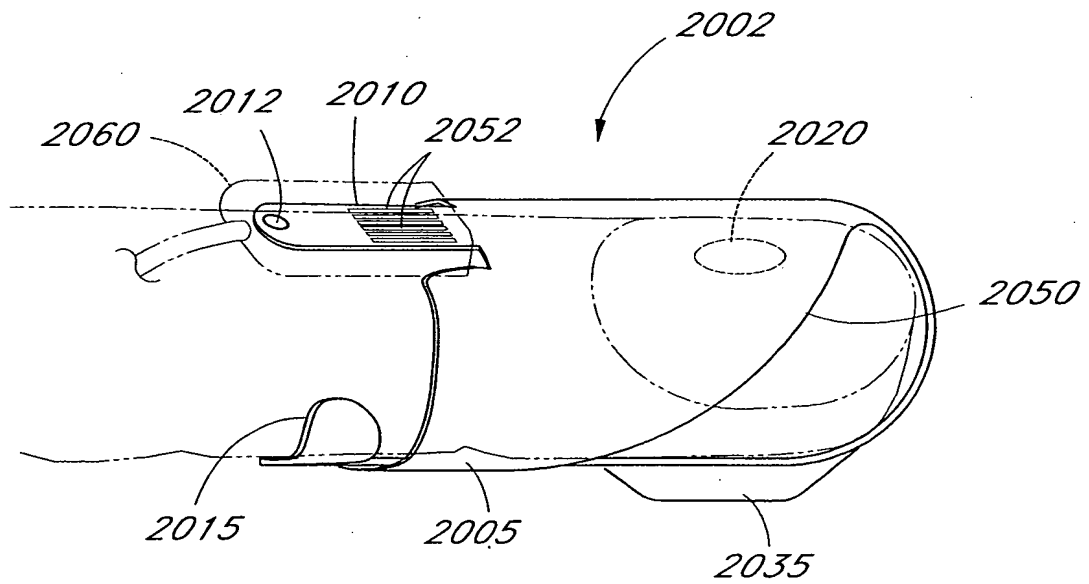
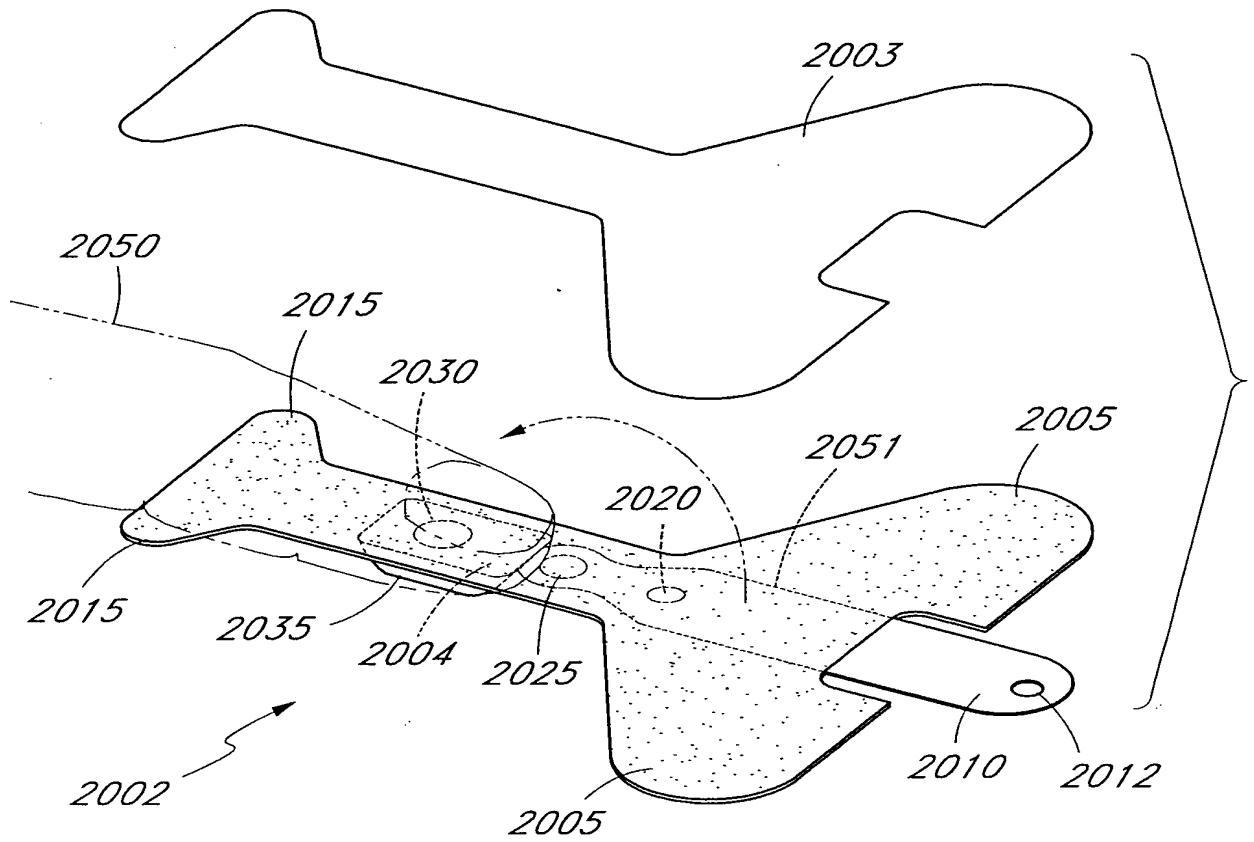


FIG. 29B

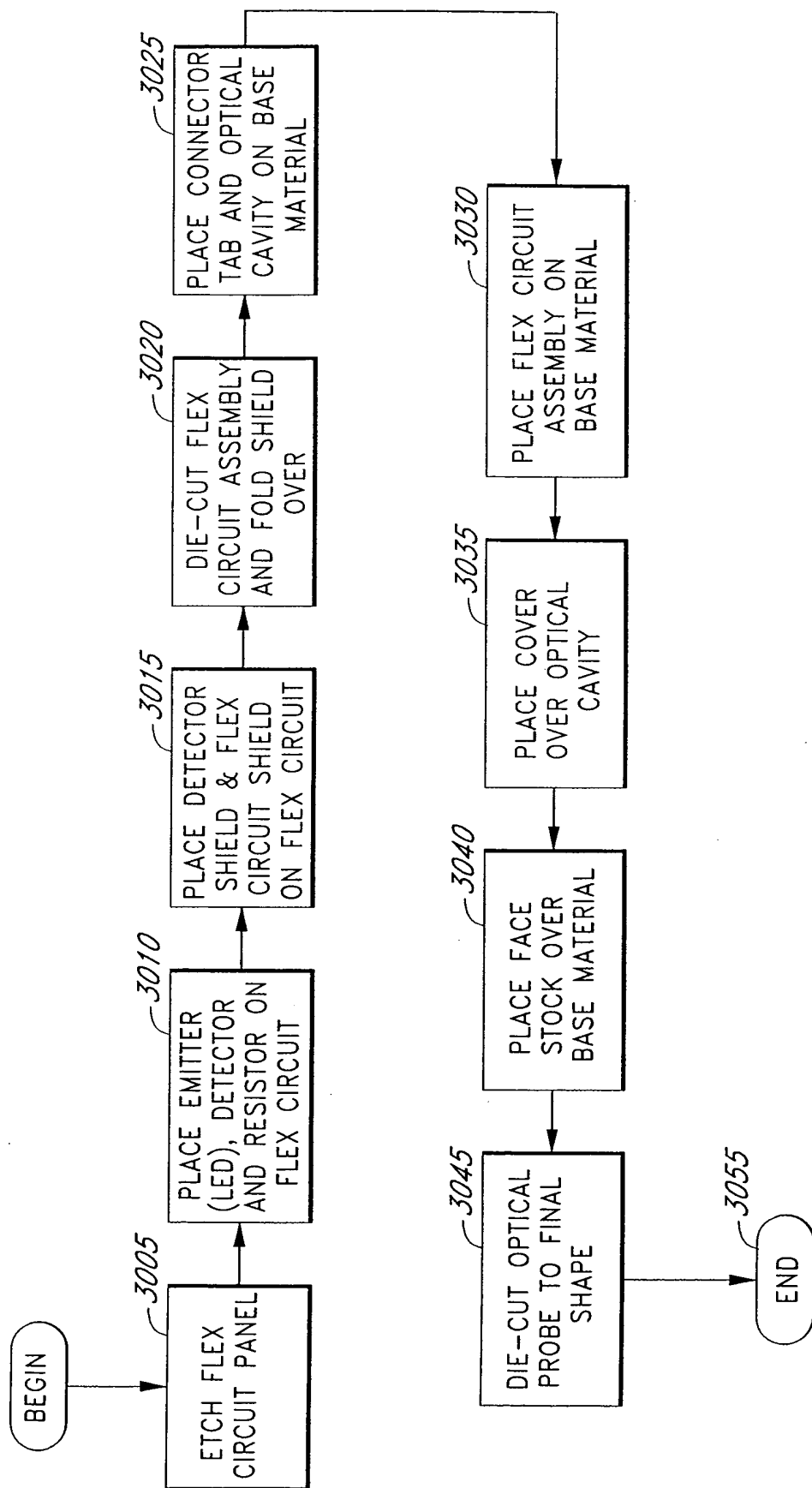


FIG. 30

FIG. 31

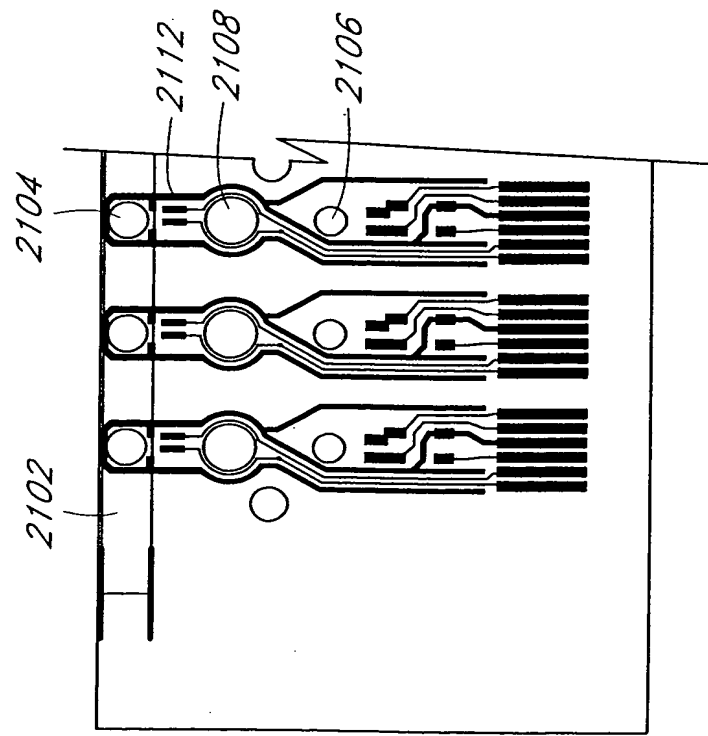


FIG. 31A

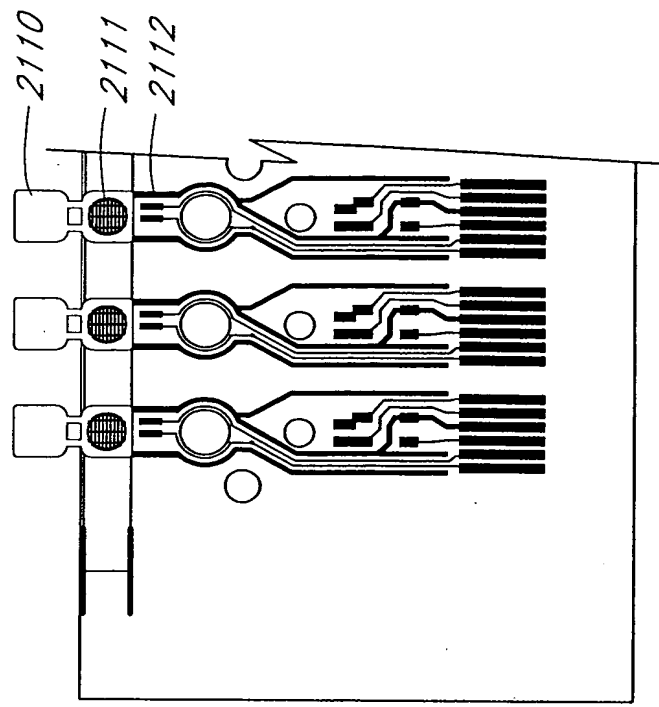


FIG. 31B

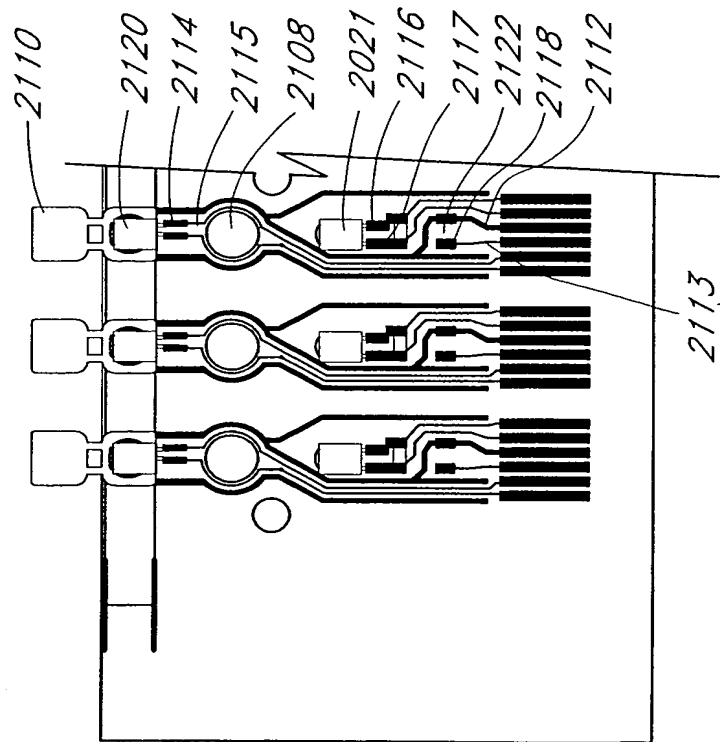


FIG. 32A

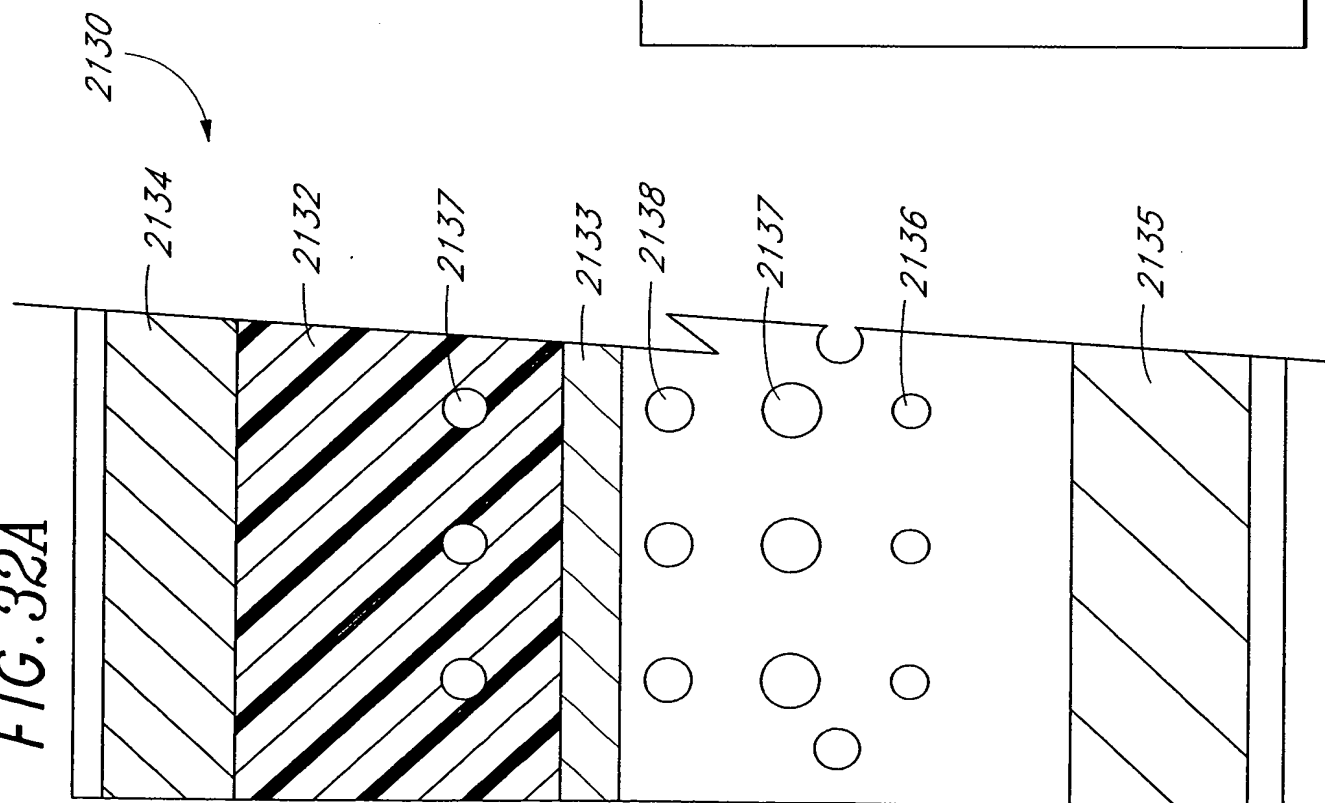
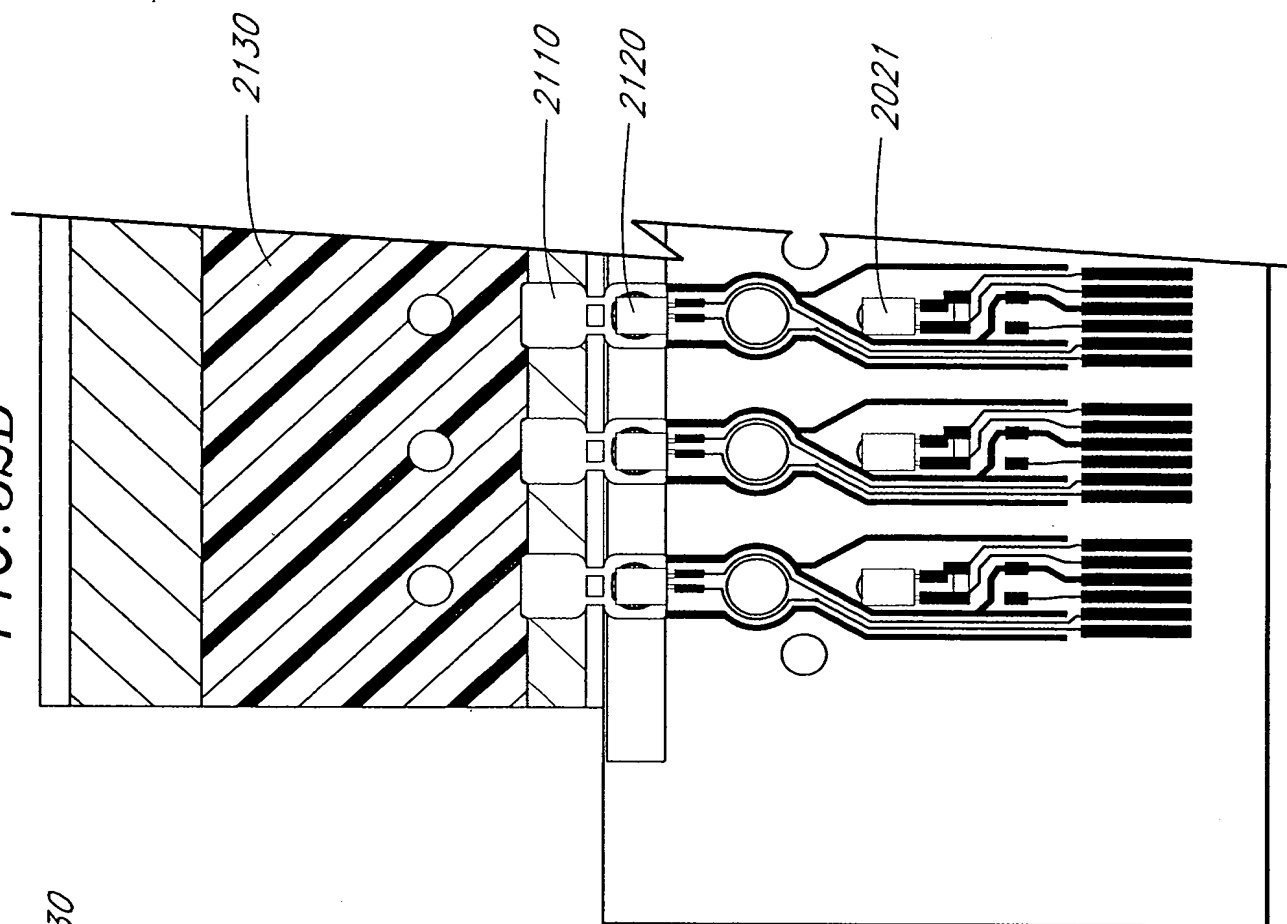


FIG. 32B



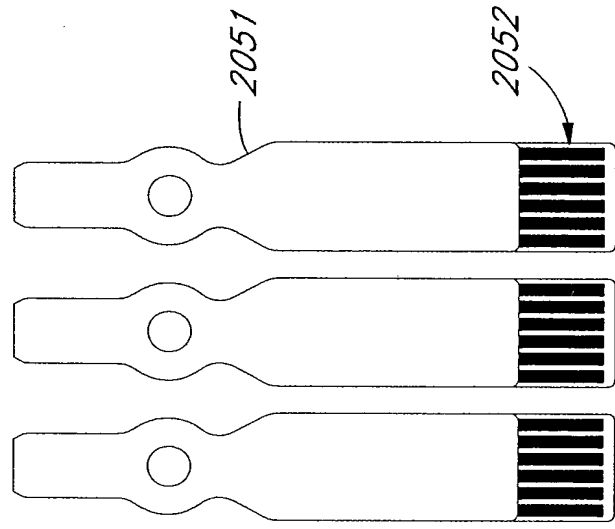
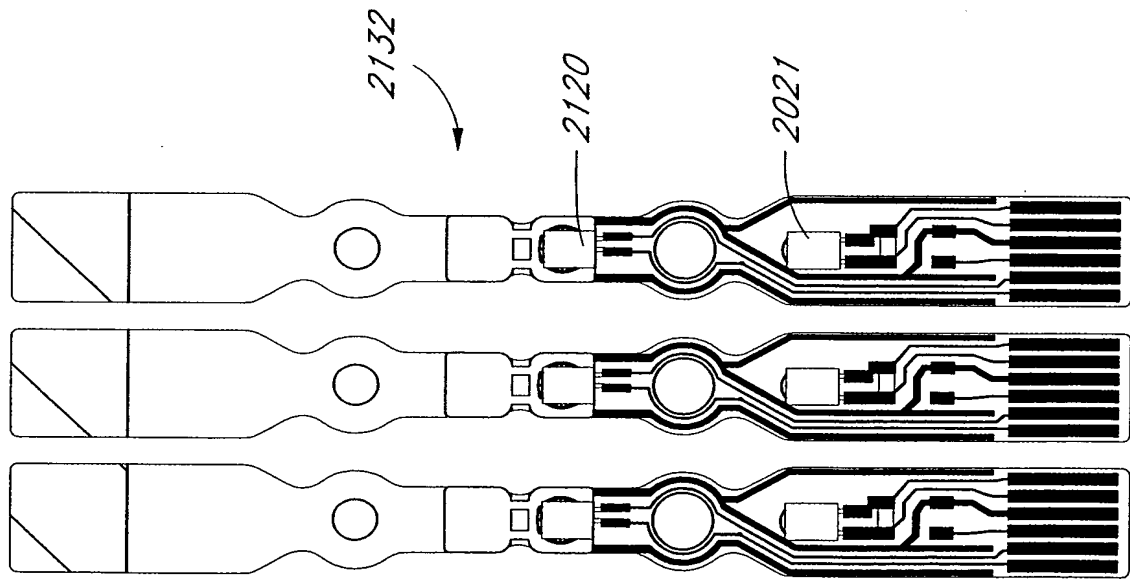


FIG. 33B

FIG. 34

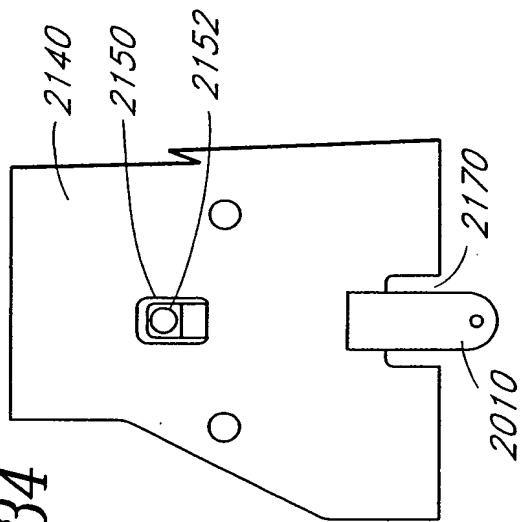


FIG. 35

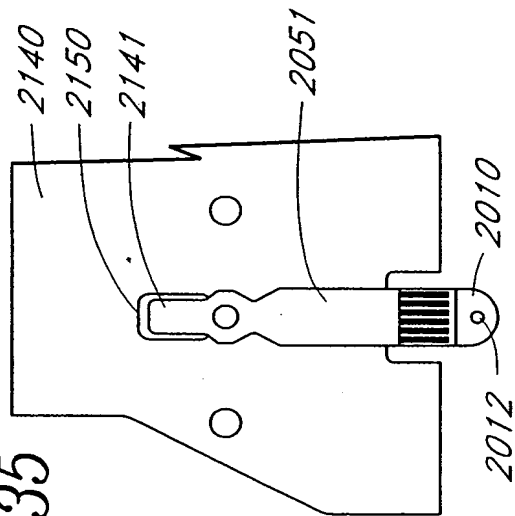


FIG. 36

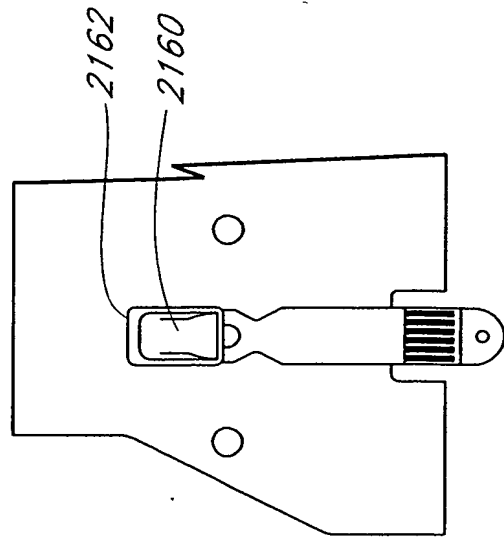


FIG. 37

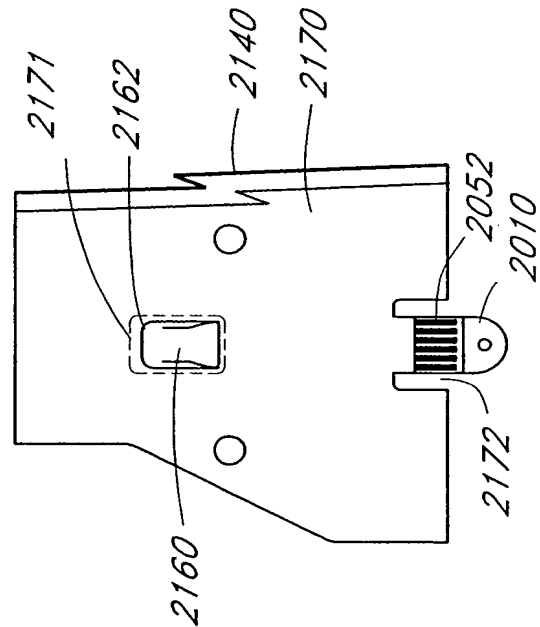


FIG. 38

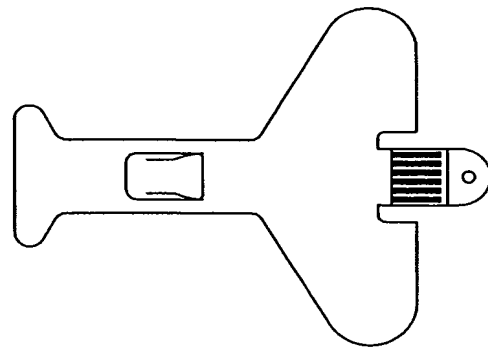


FIG. 39A

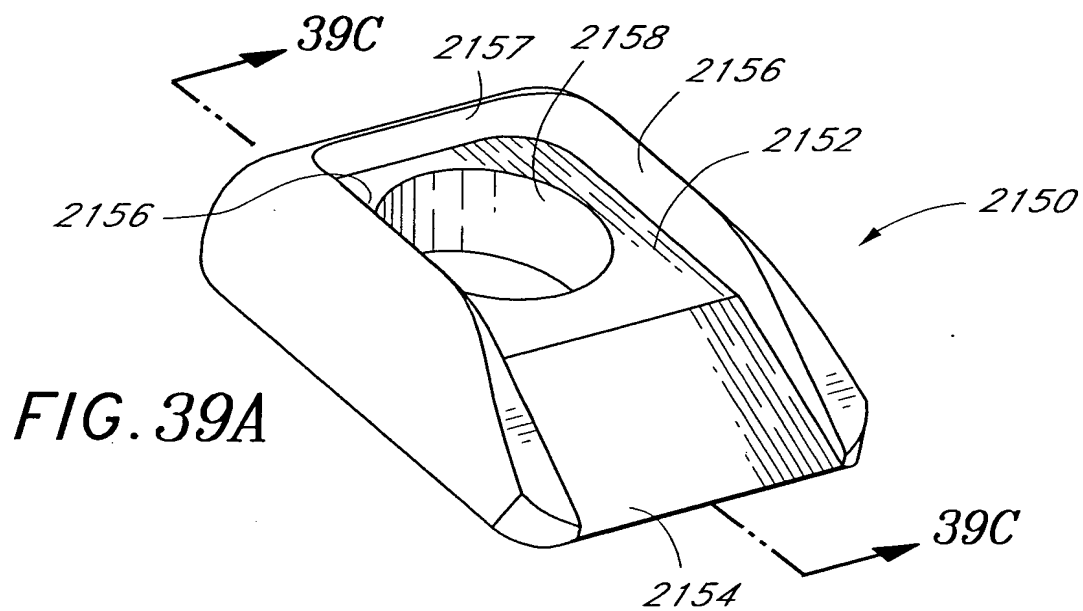


FIG. 39B

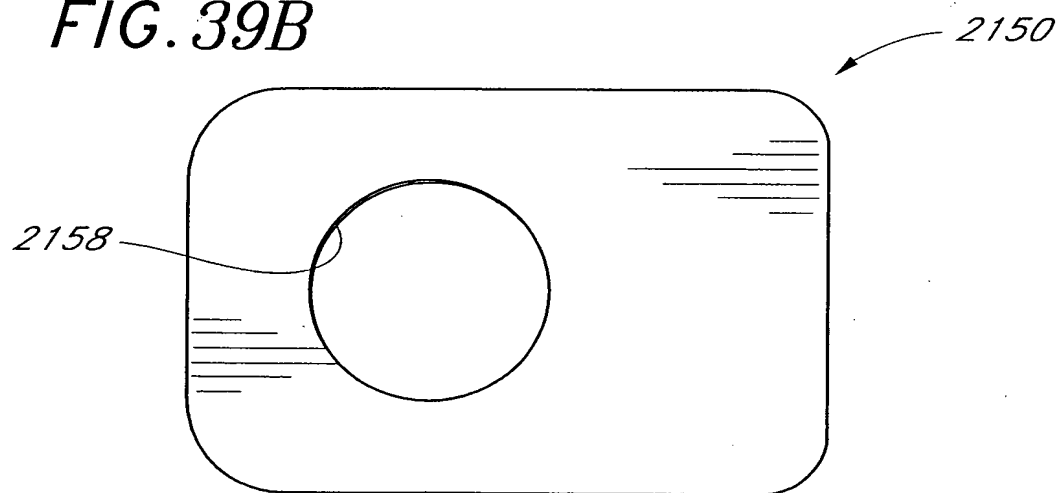
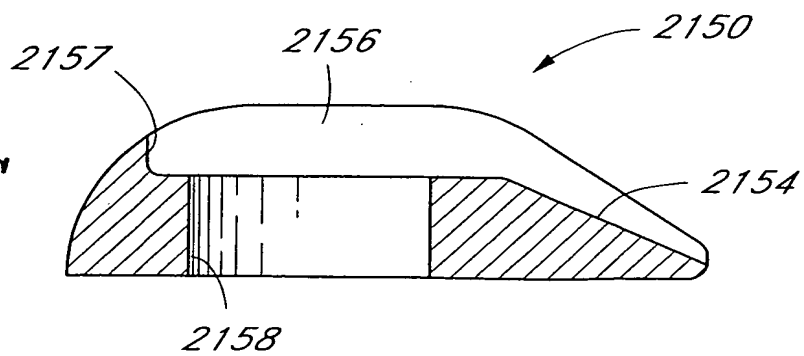


FIG. 39C



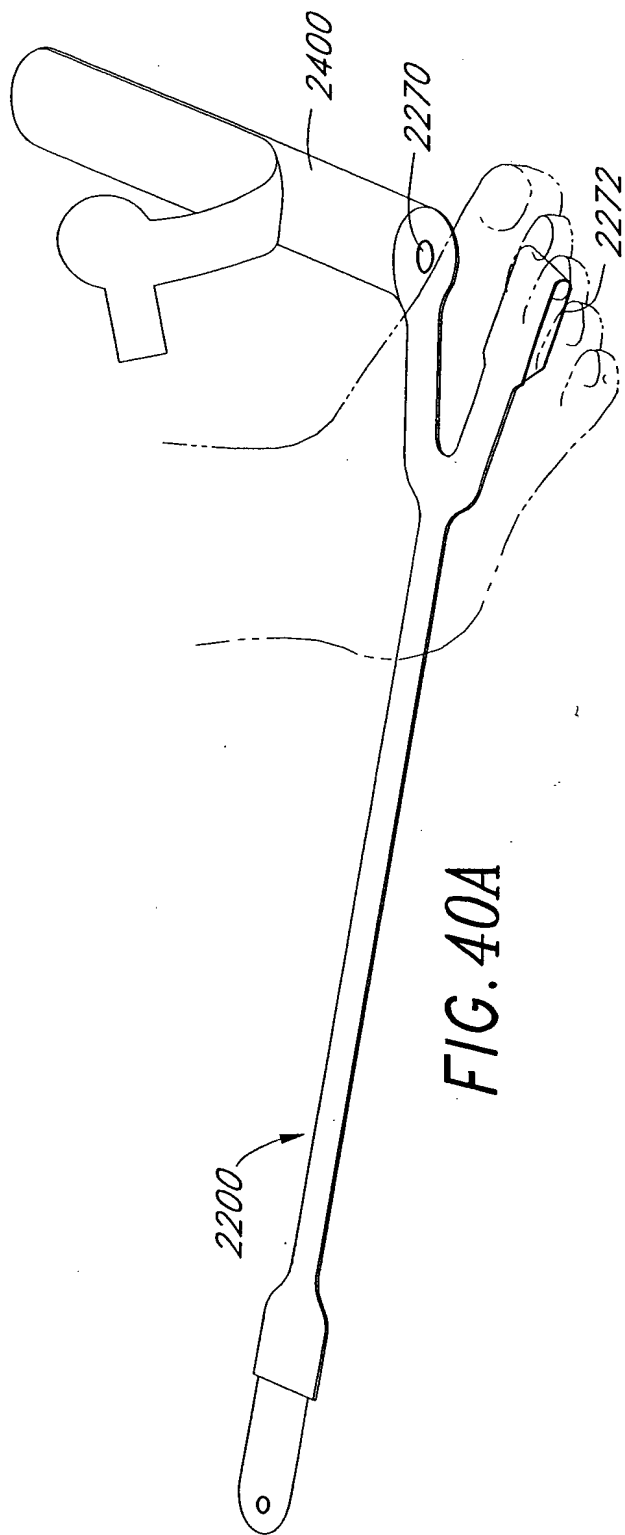


FIG. 40A

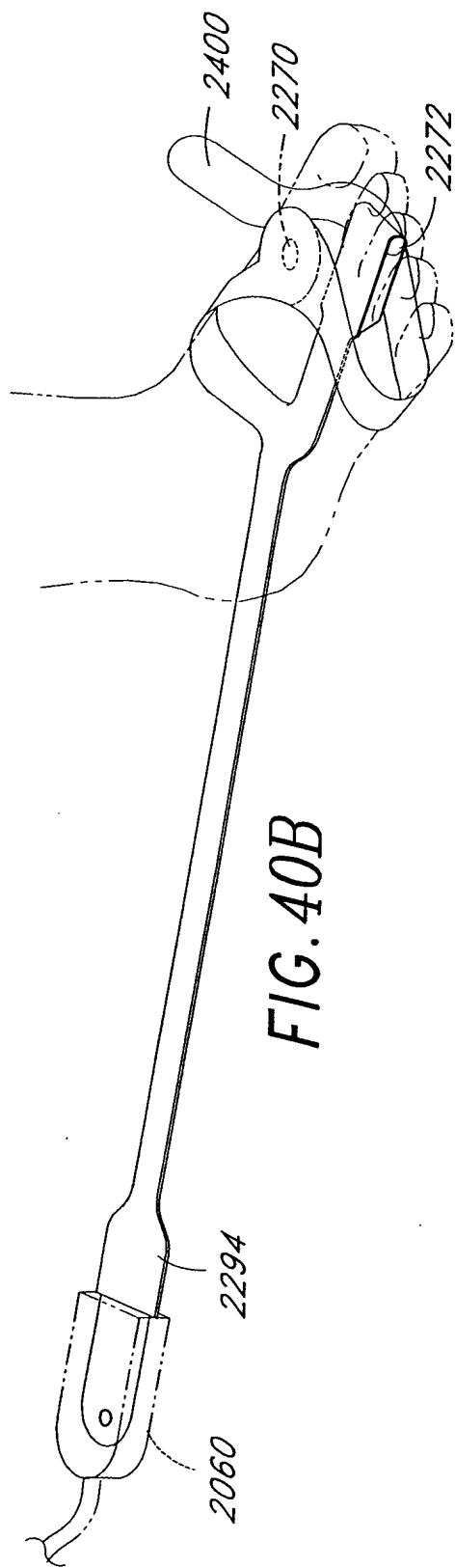


FIG. 40B

FIG. 41

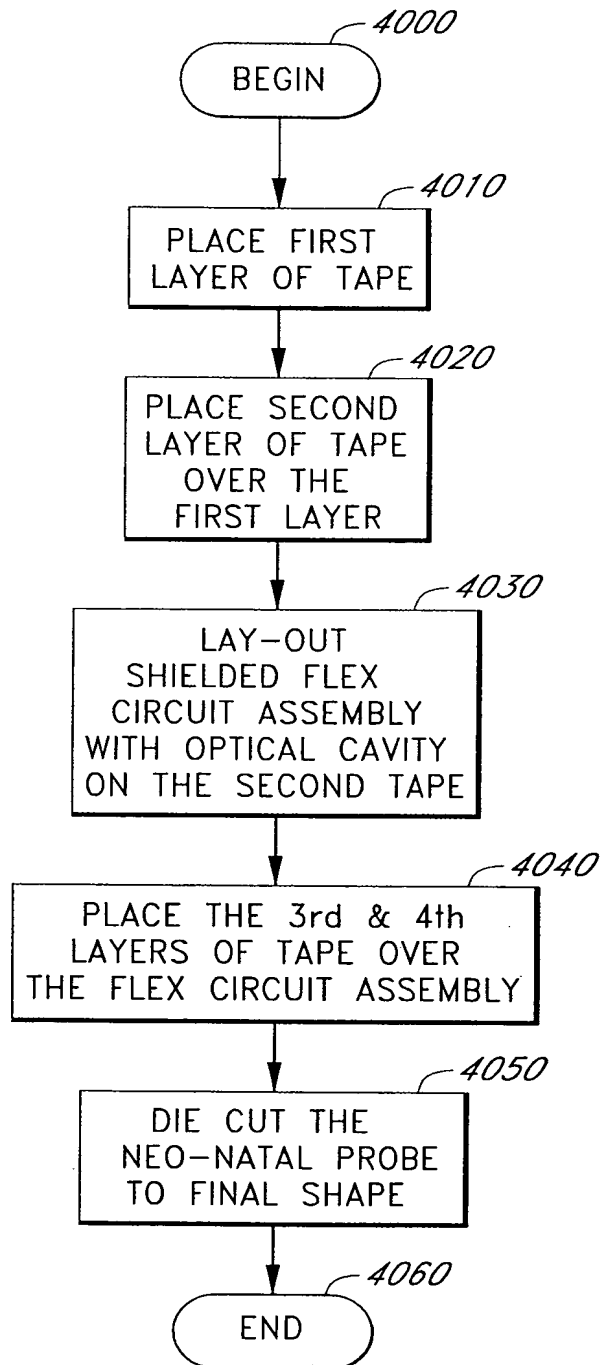


FIG. 42

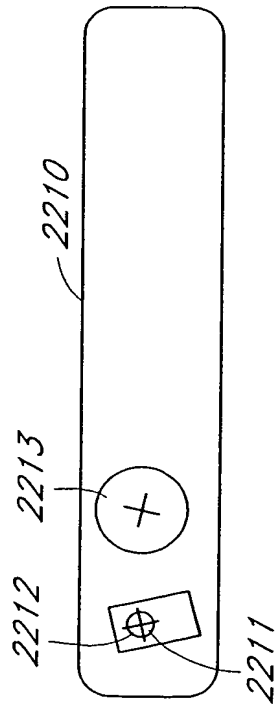
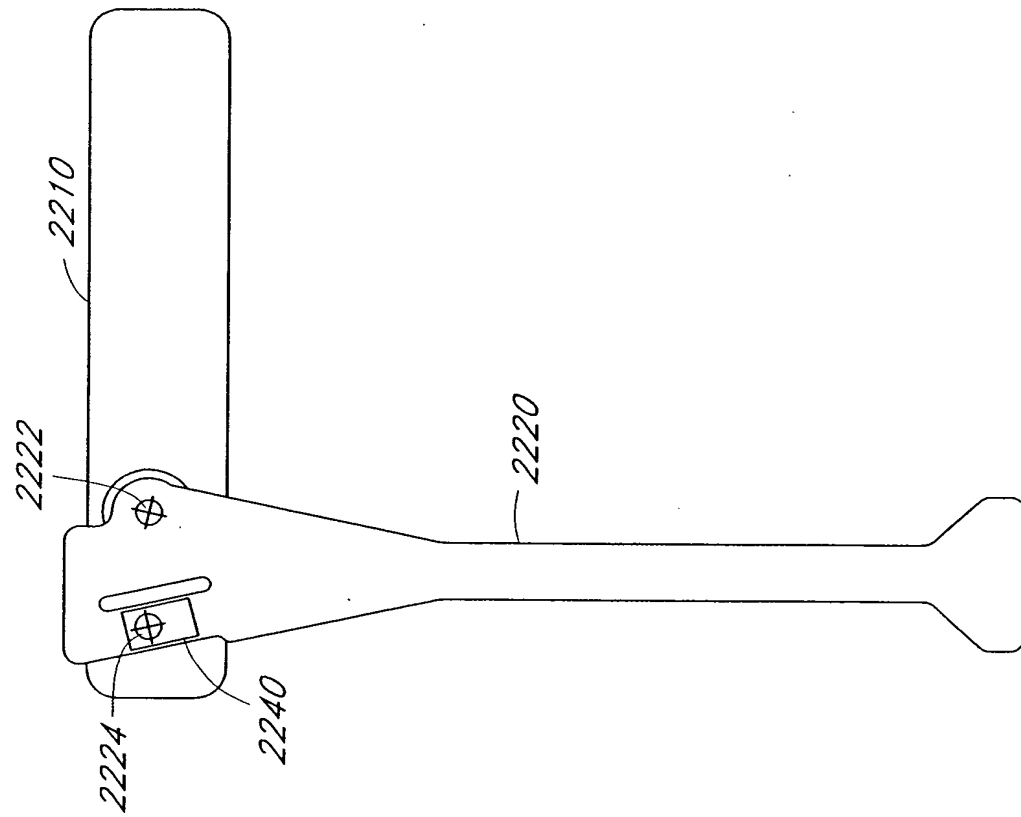


FIG. 43



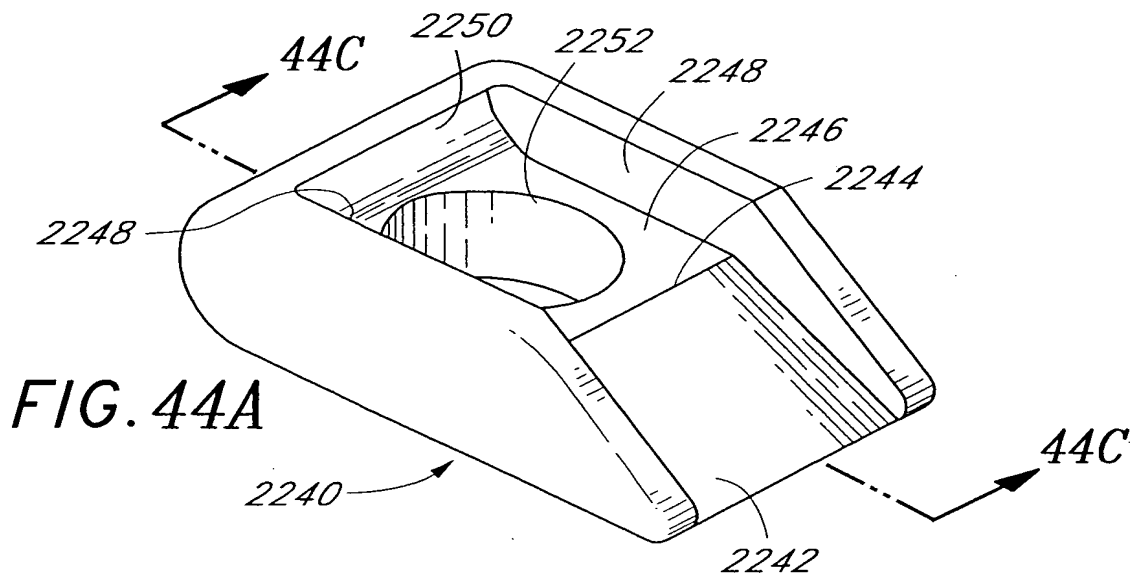
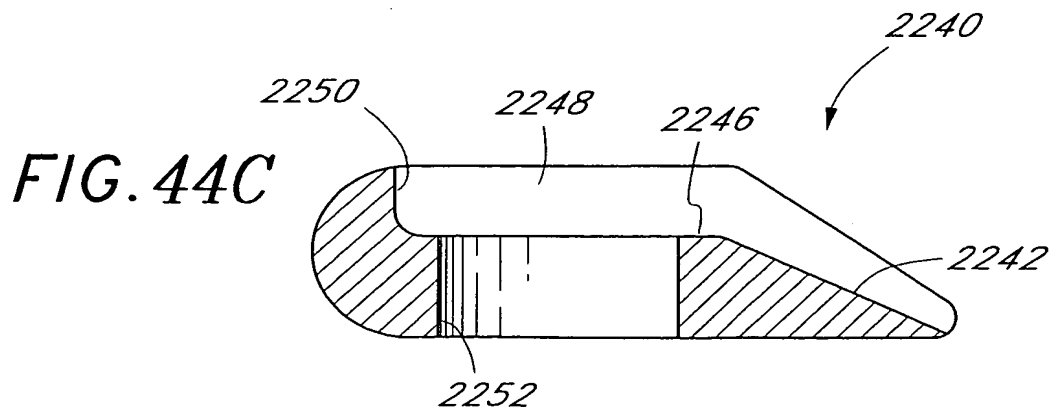
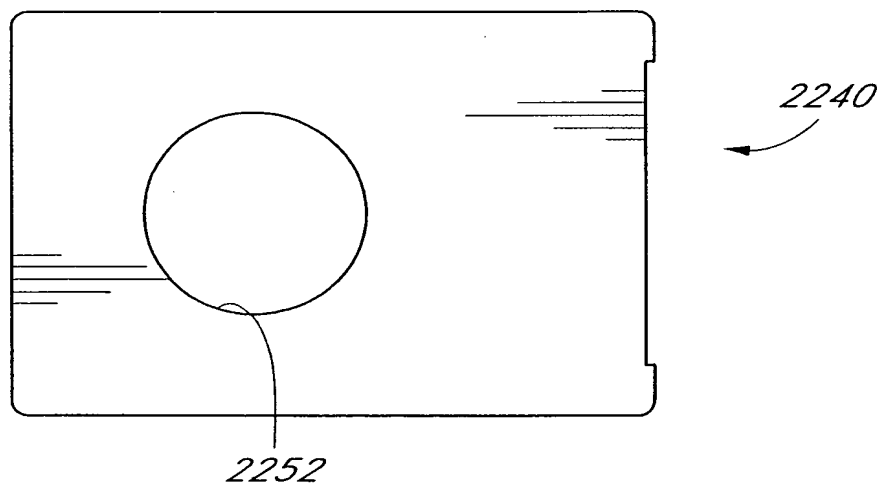


FIG. 44B



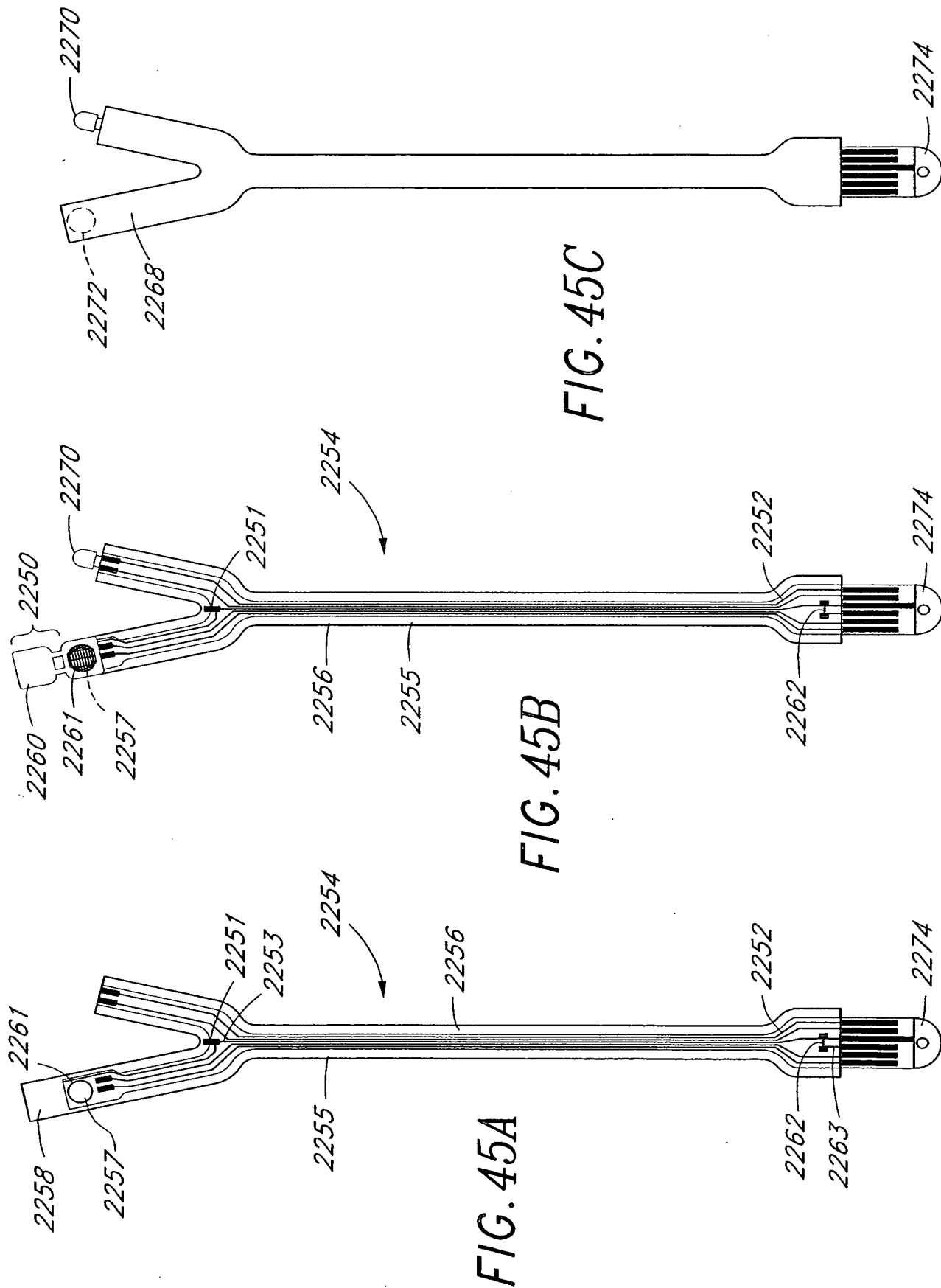


FIG. 46

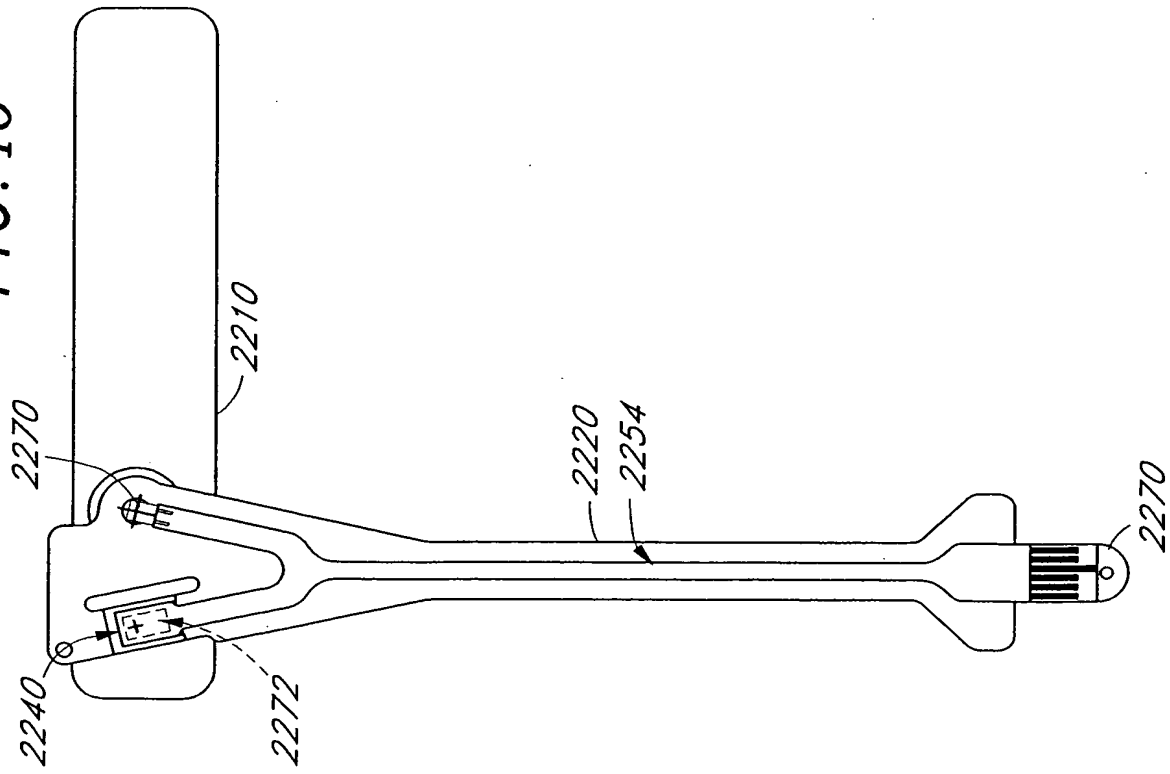


FIG. 47

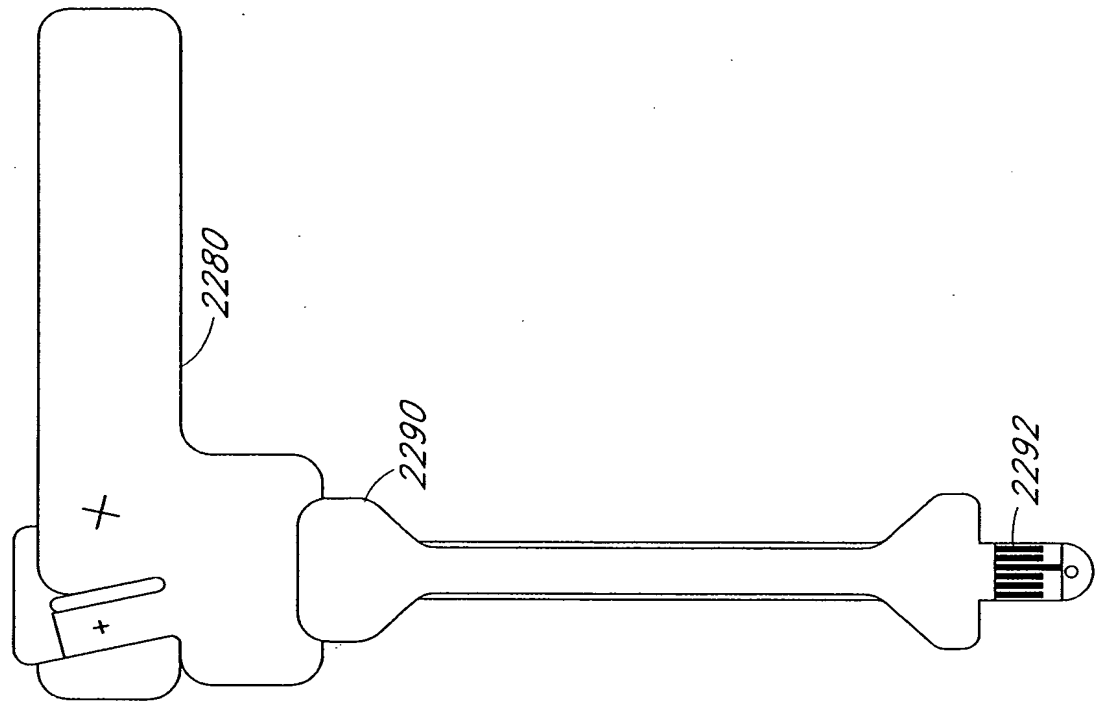


FIG. 48

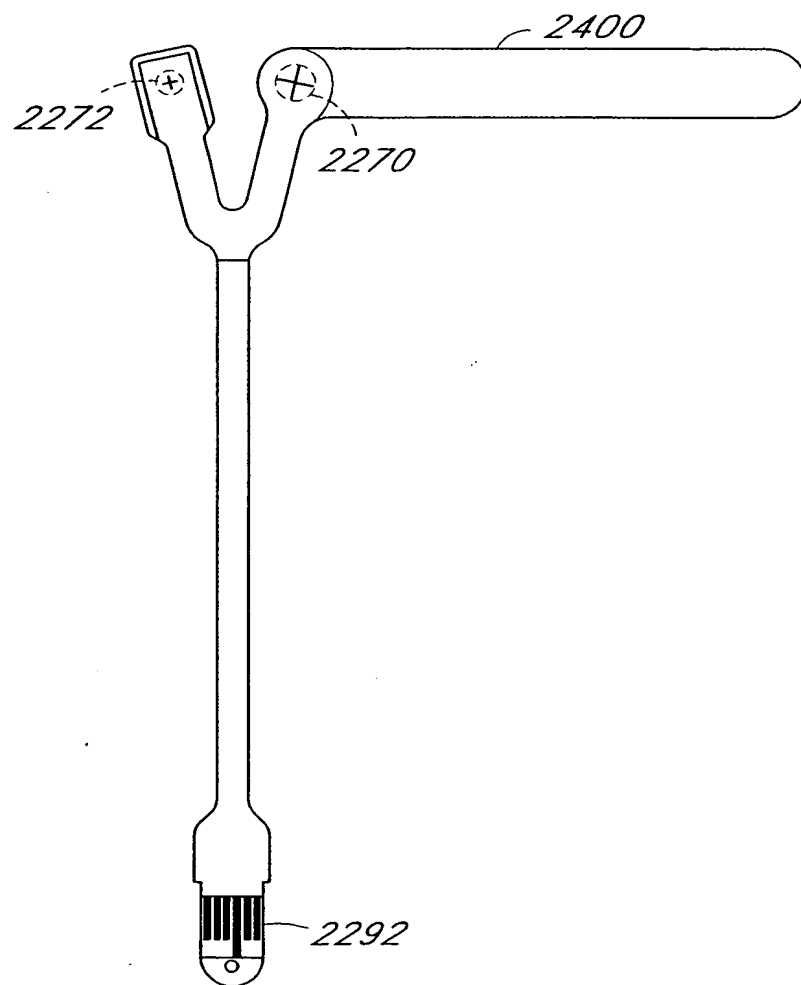


FIG. 49

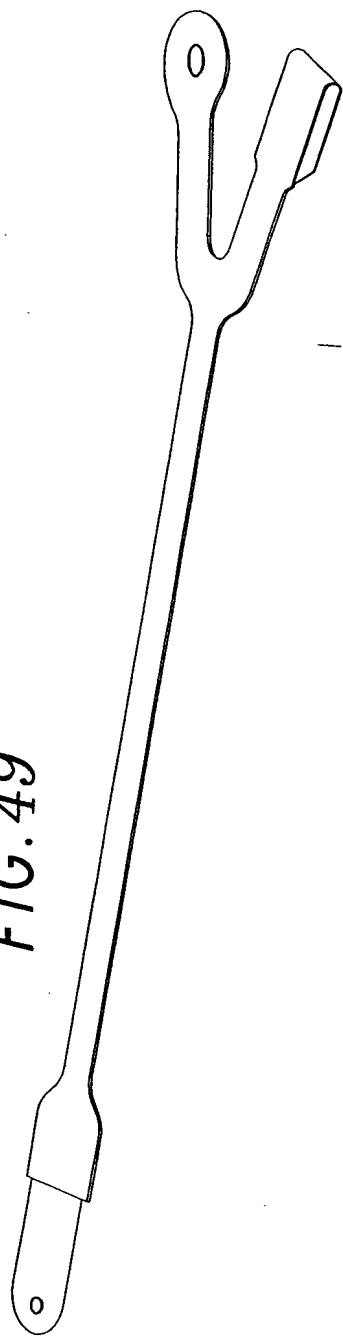
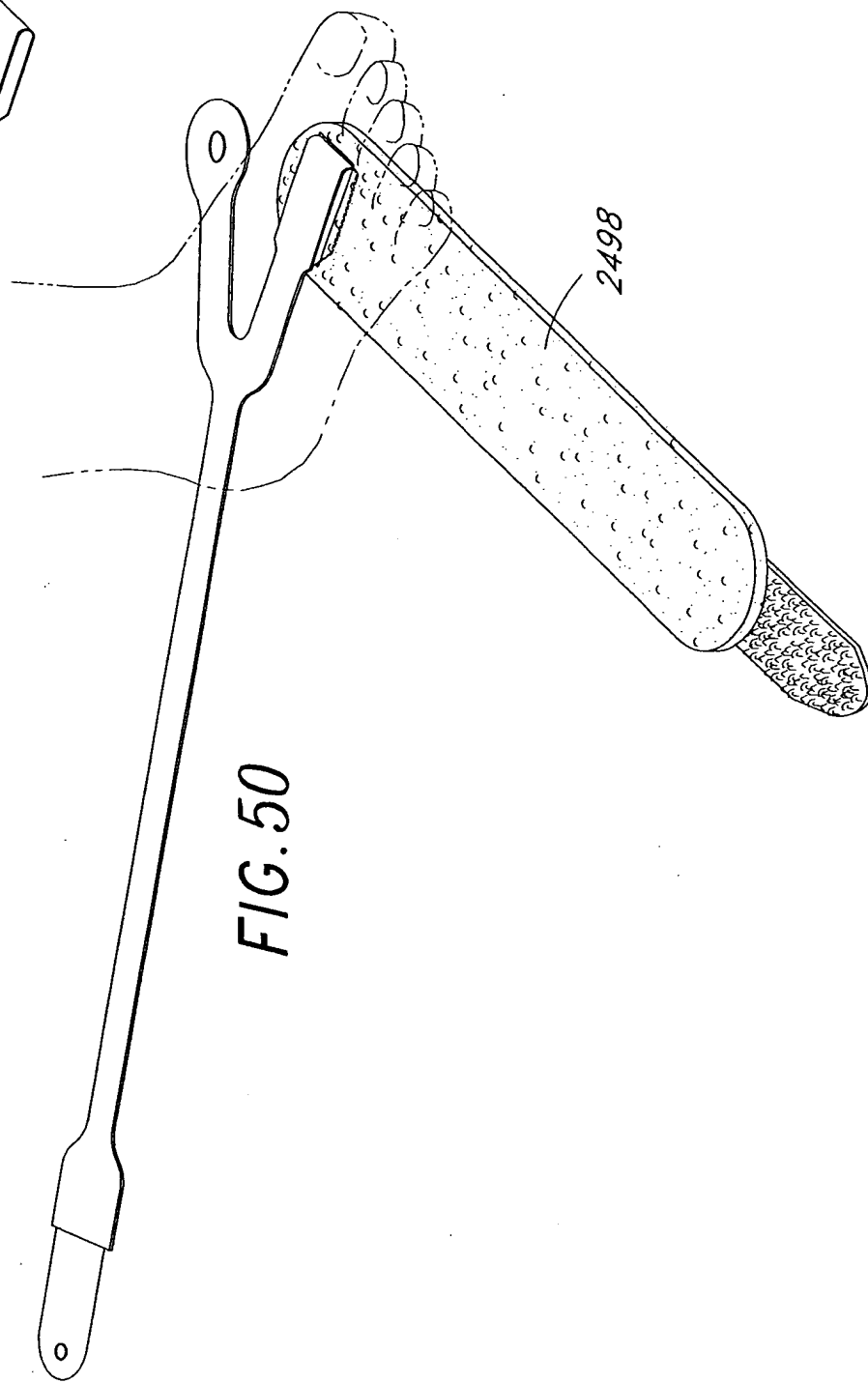


FIG. 50



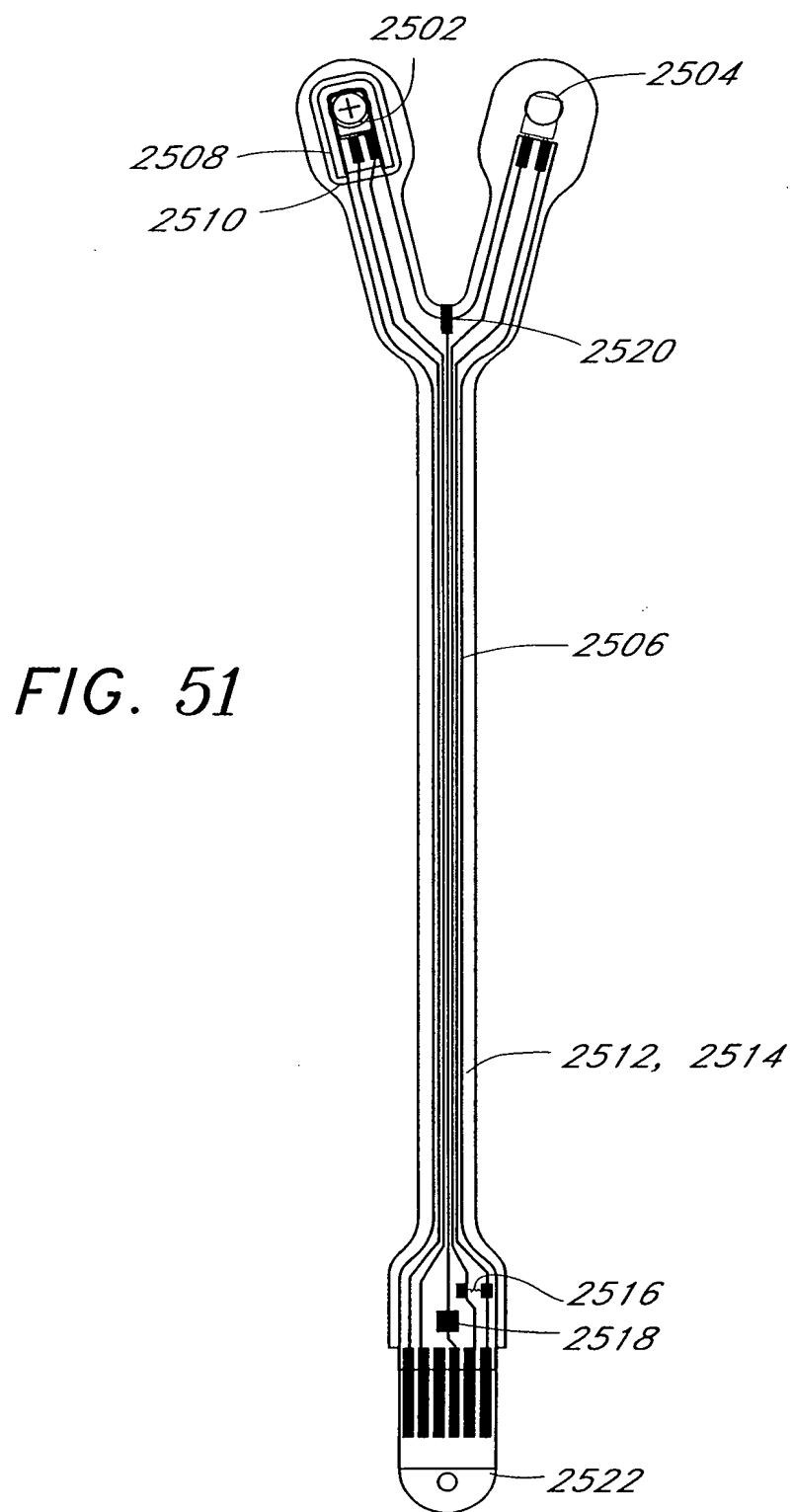


FIG. 52A

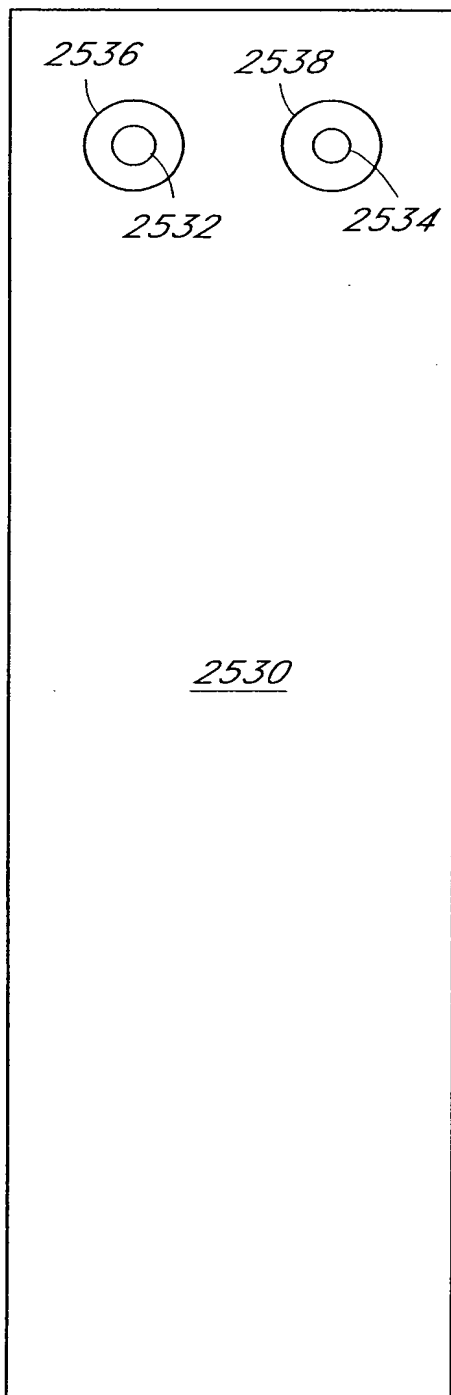


FIG. 52B

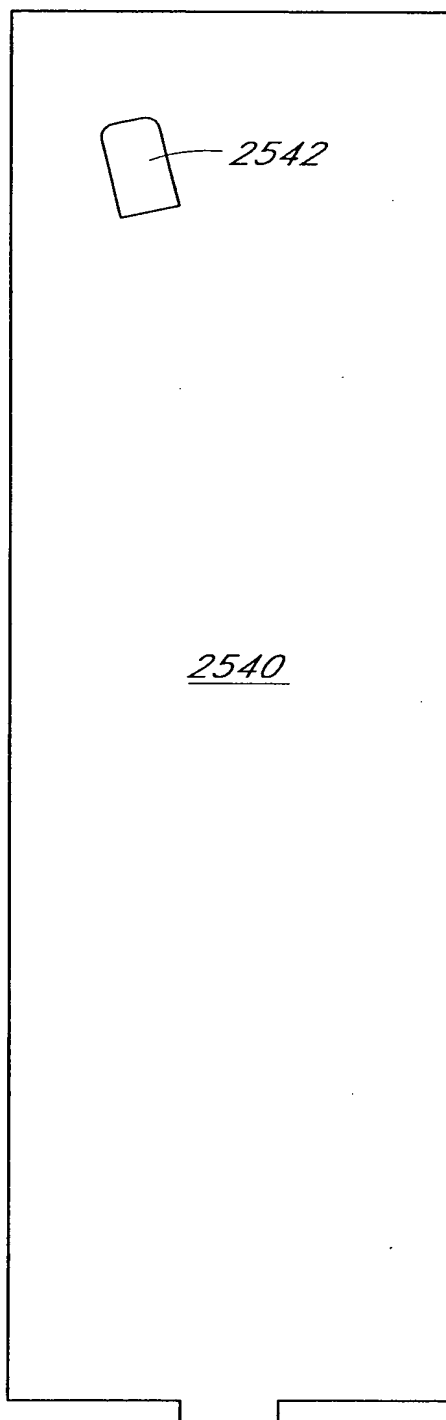


FIG. 53A

FIG. 53B

FIG. 54

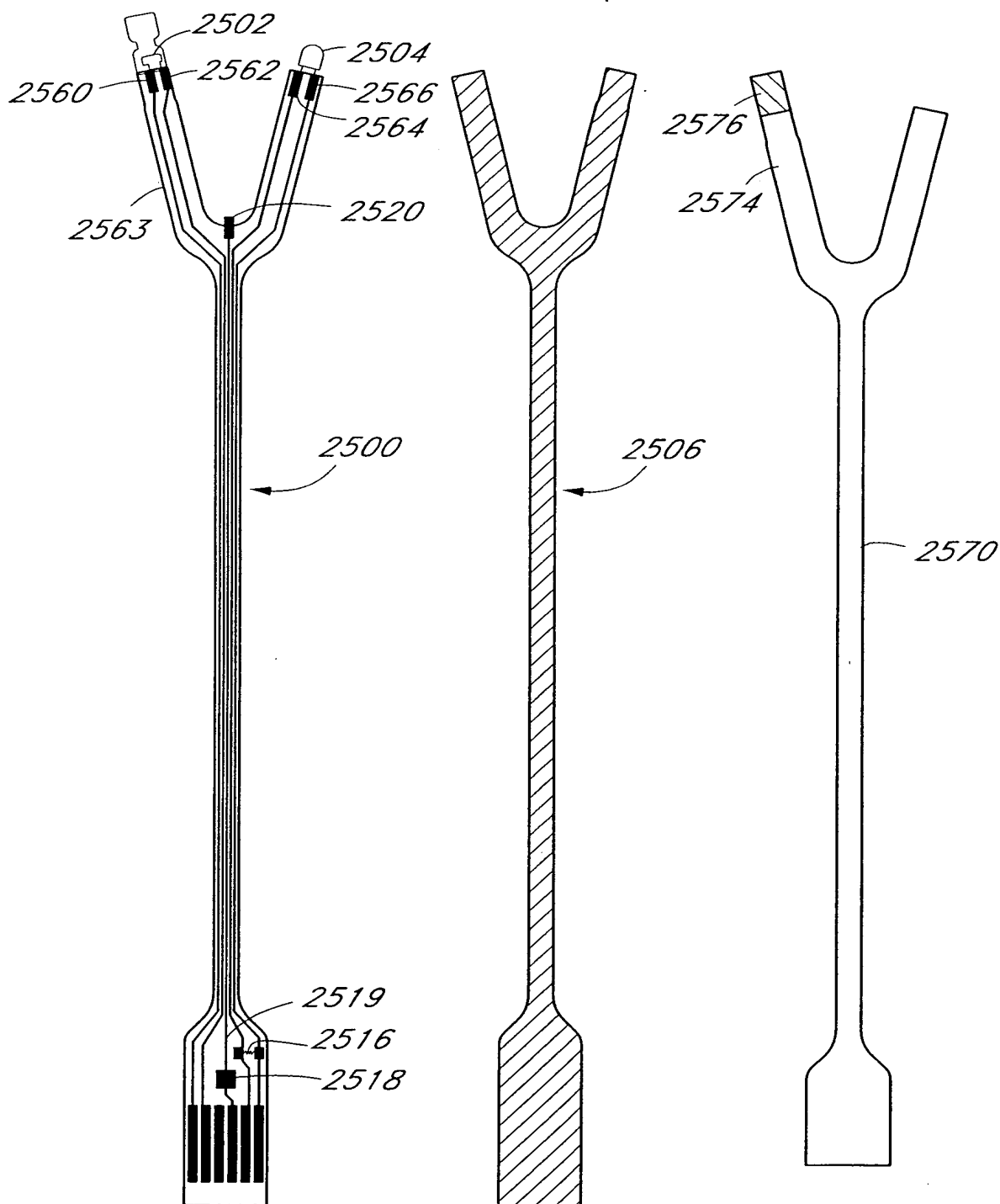


FIG. 55A

2510

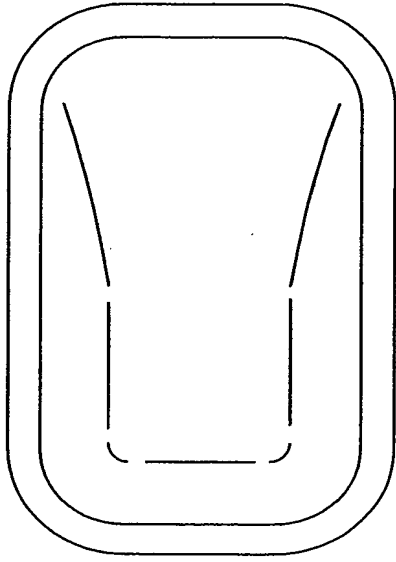


FIG. 55B

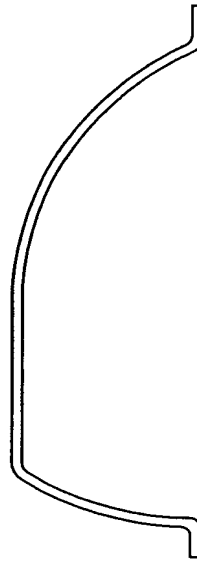
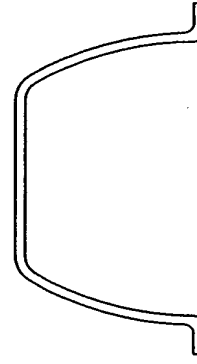


FIG. 55C



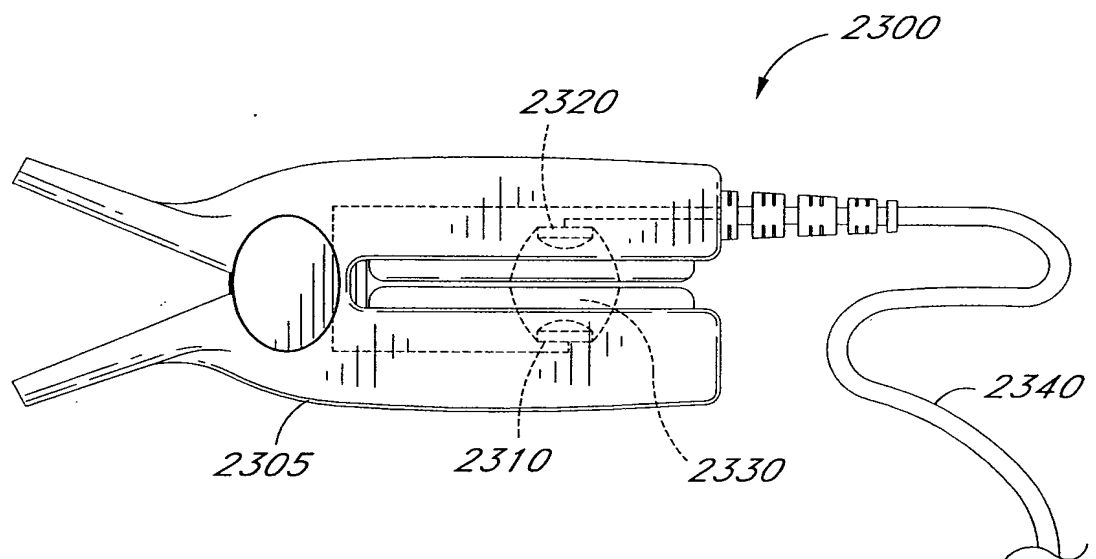


FIG. 56